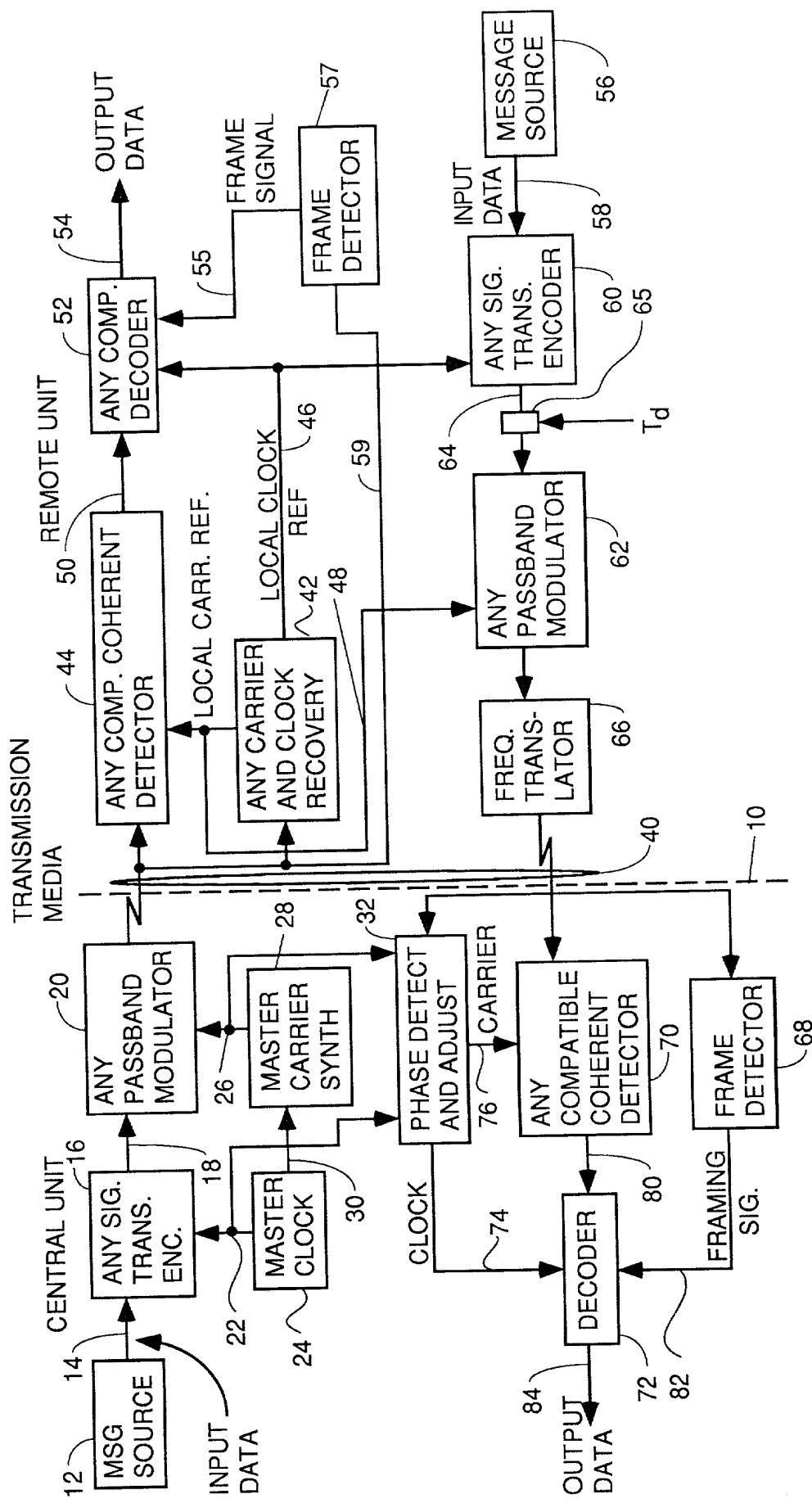


FIG. 1



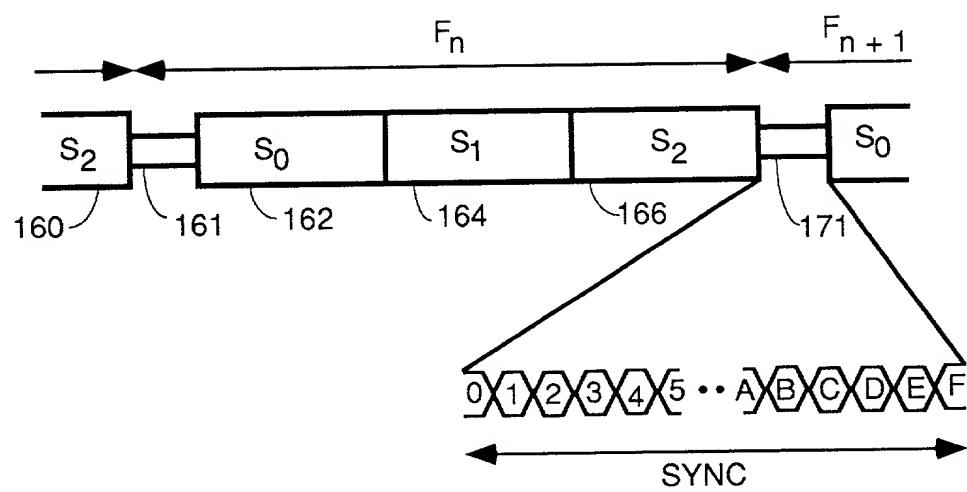


FIG. 2A

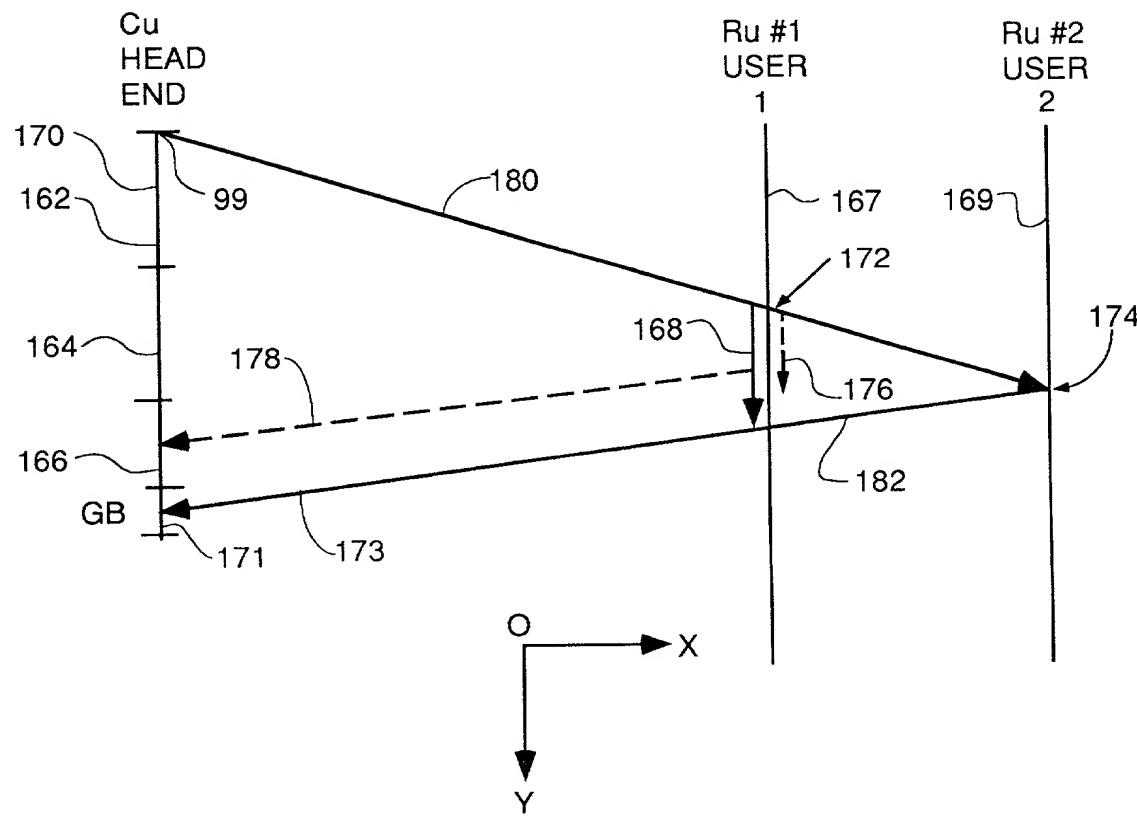


FIG. 2B

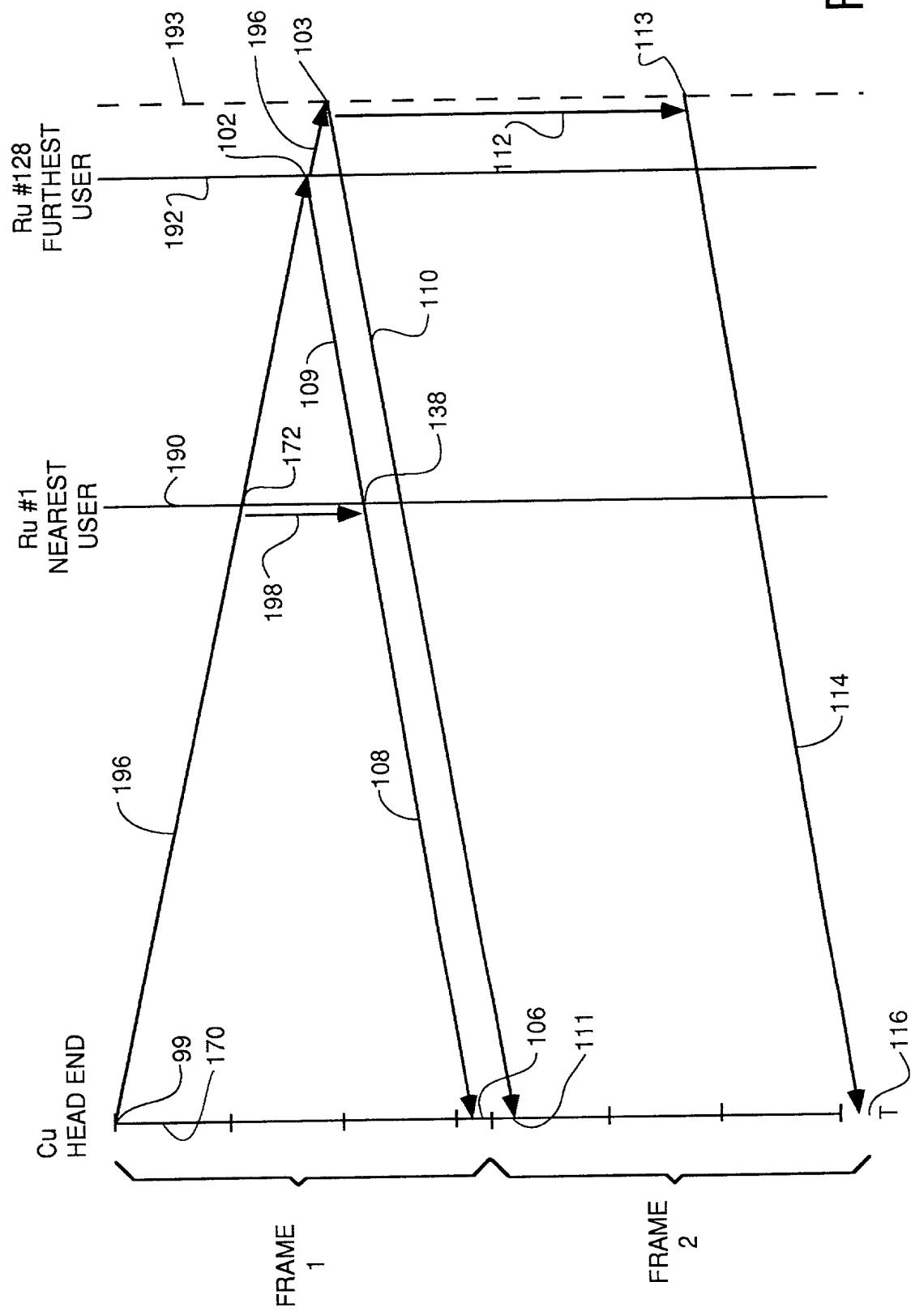


FIG. 3

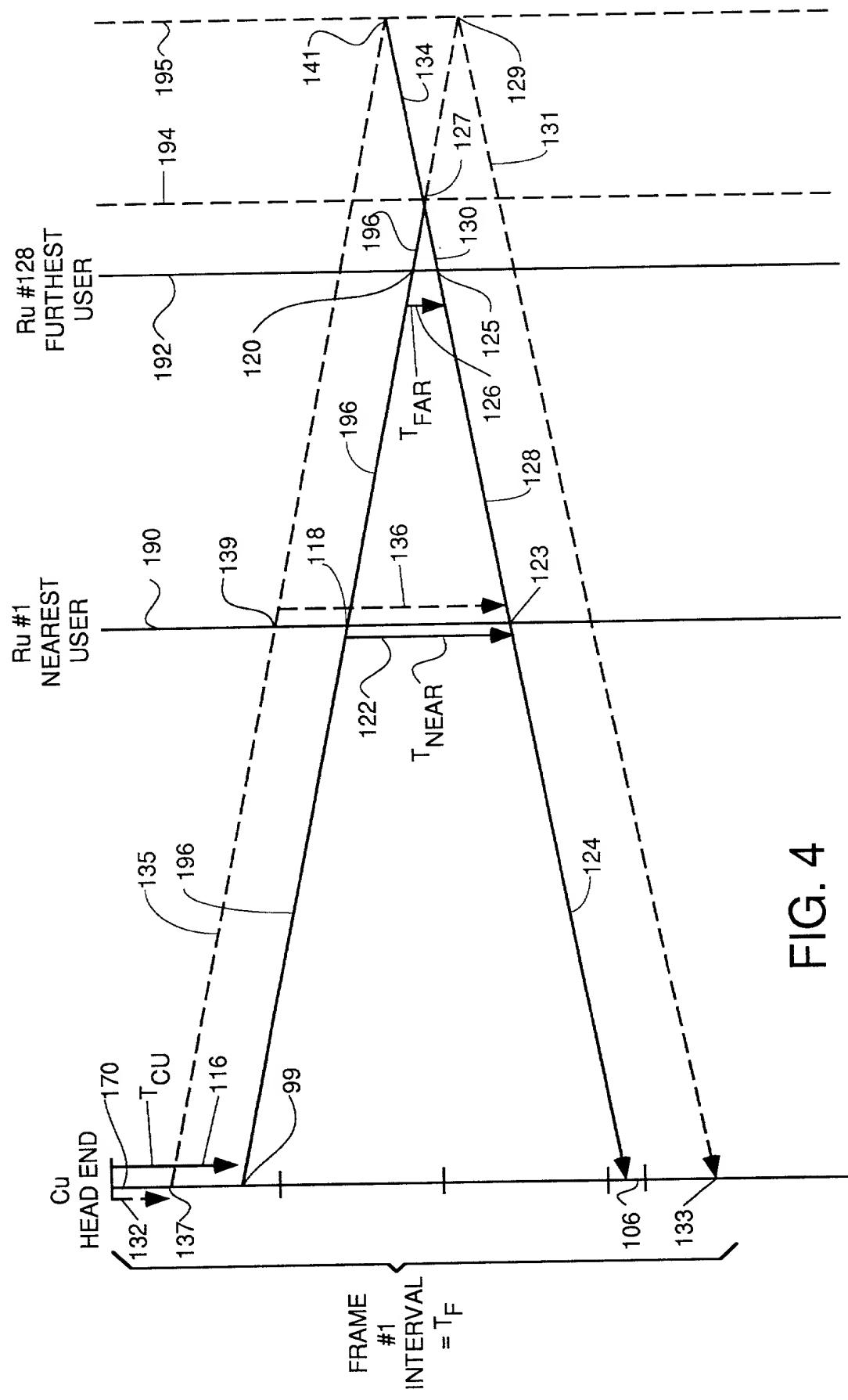
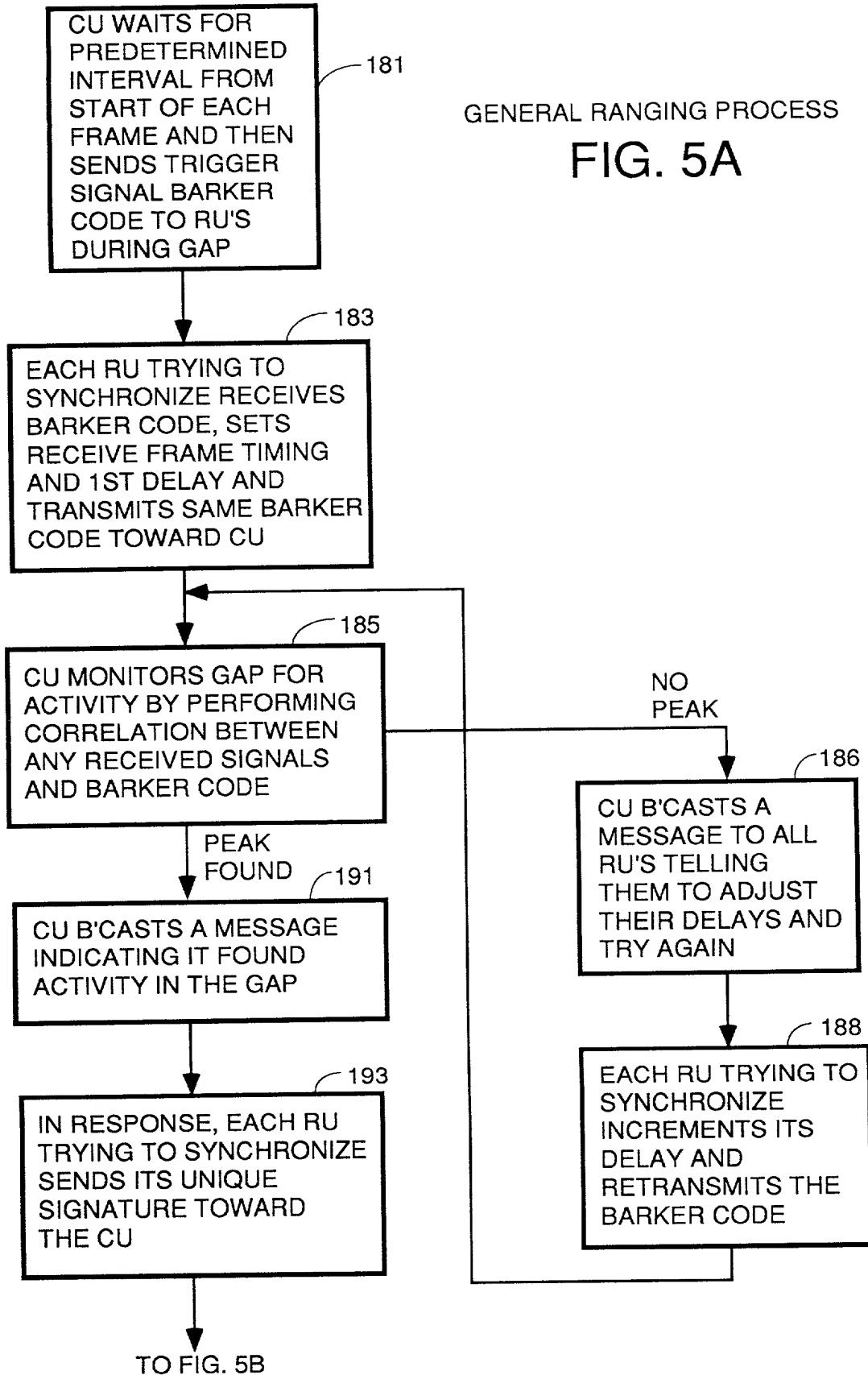


FIG. 4



000000000000000000000000

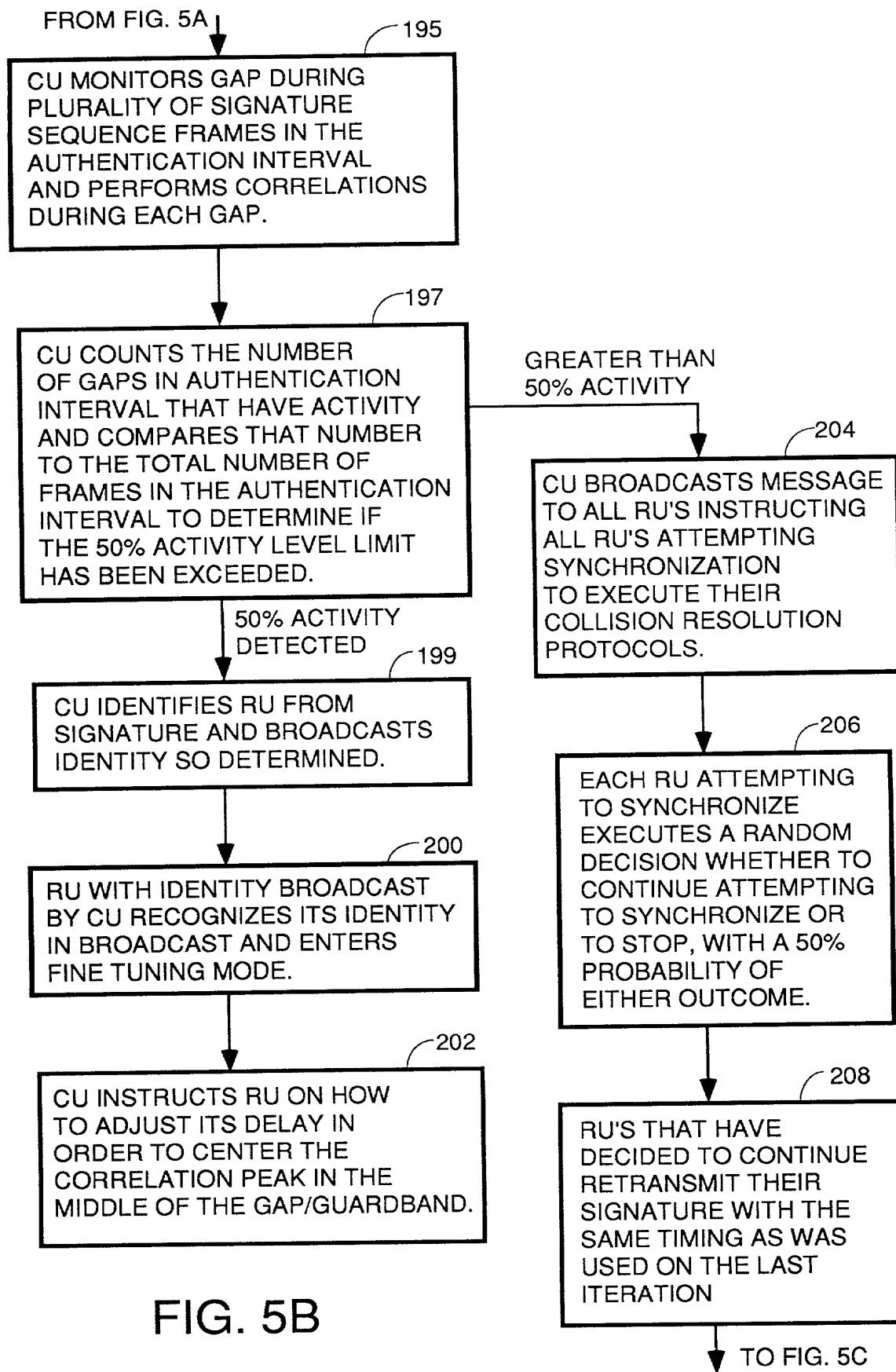


FIG. 5B

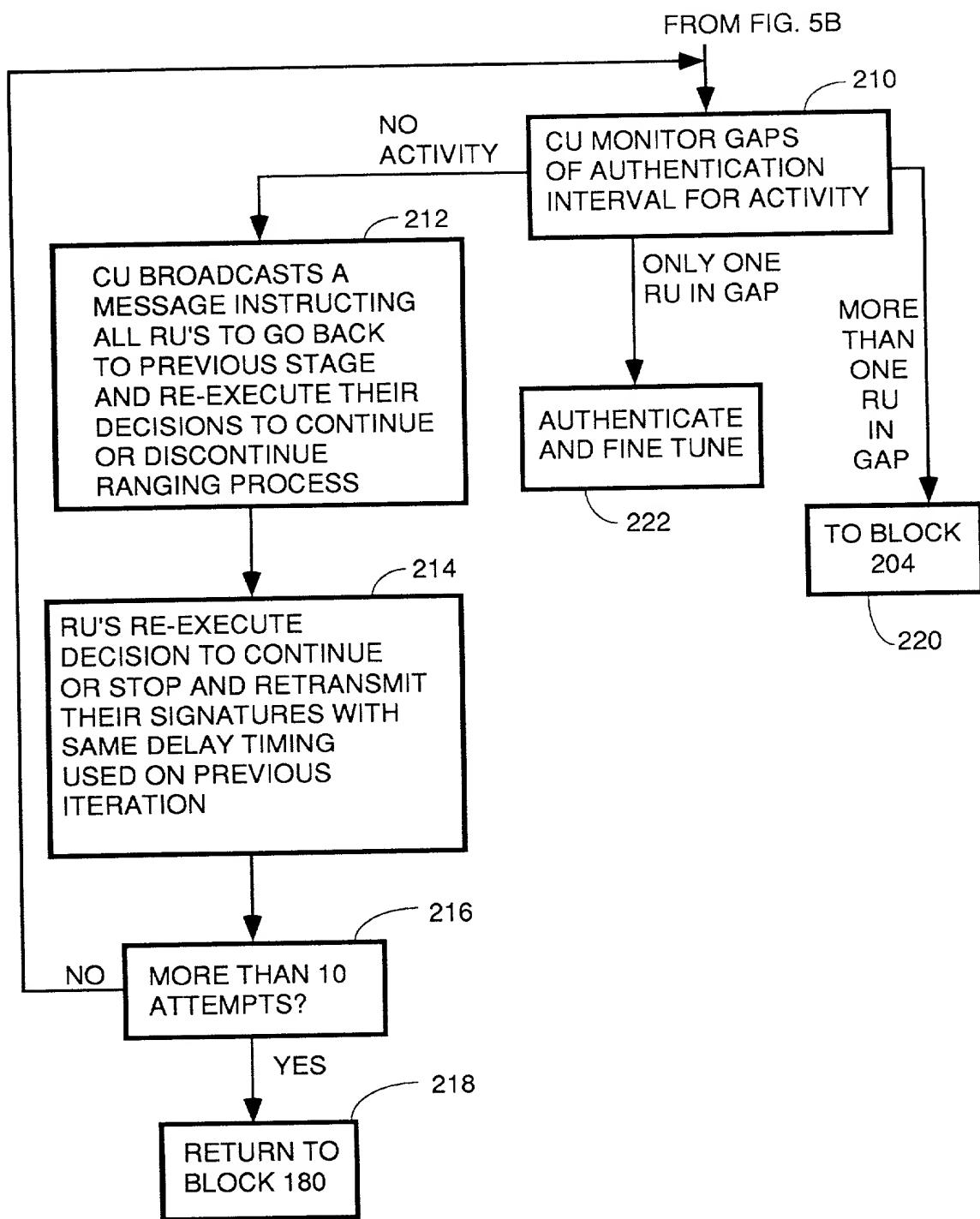


FIG. 5C

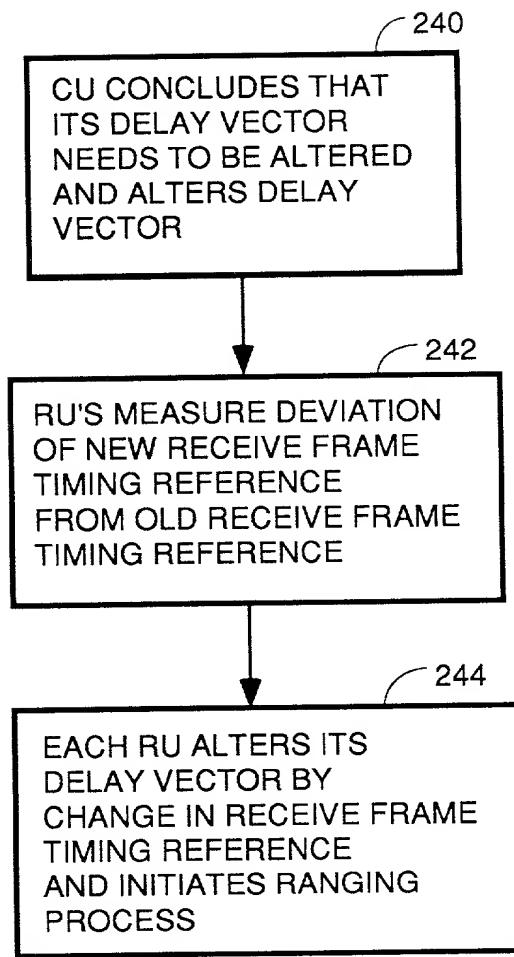


FIG. 6
DEAD RECKONING RE-SYNC

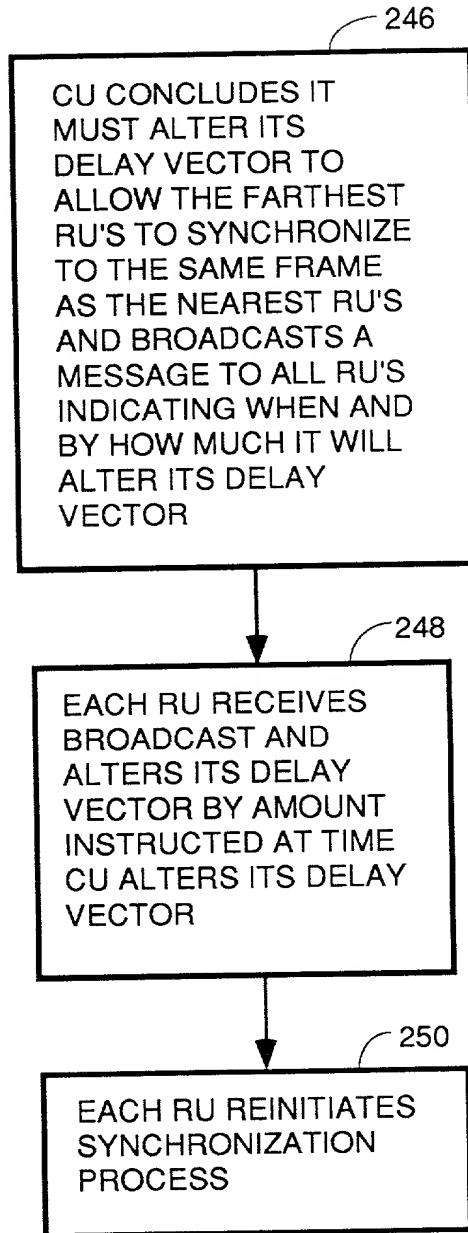


FIG. 7
PRECURSOR EMBODIMENT

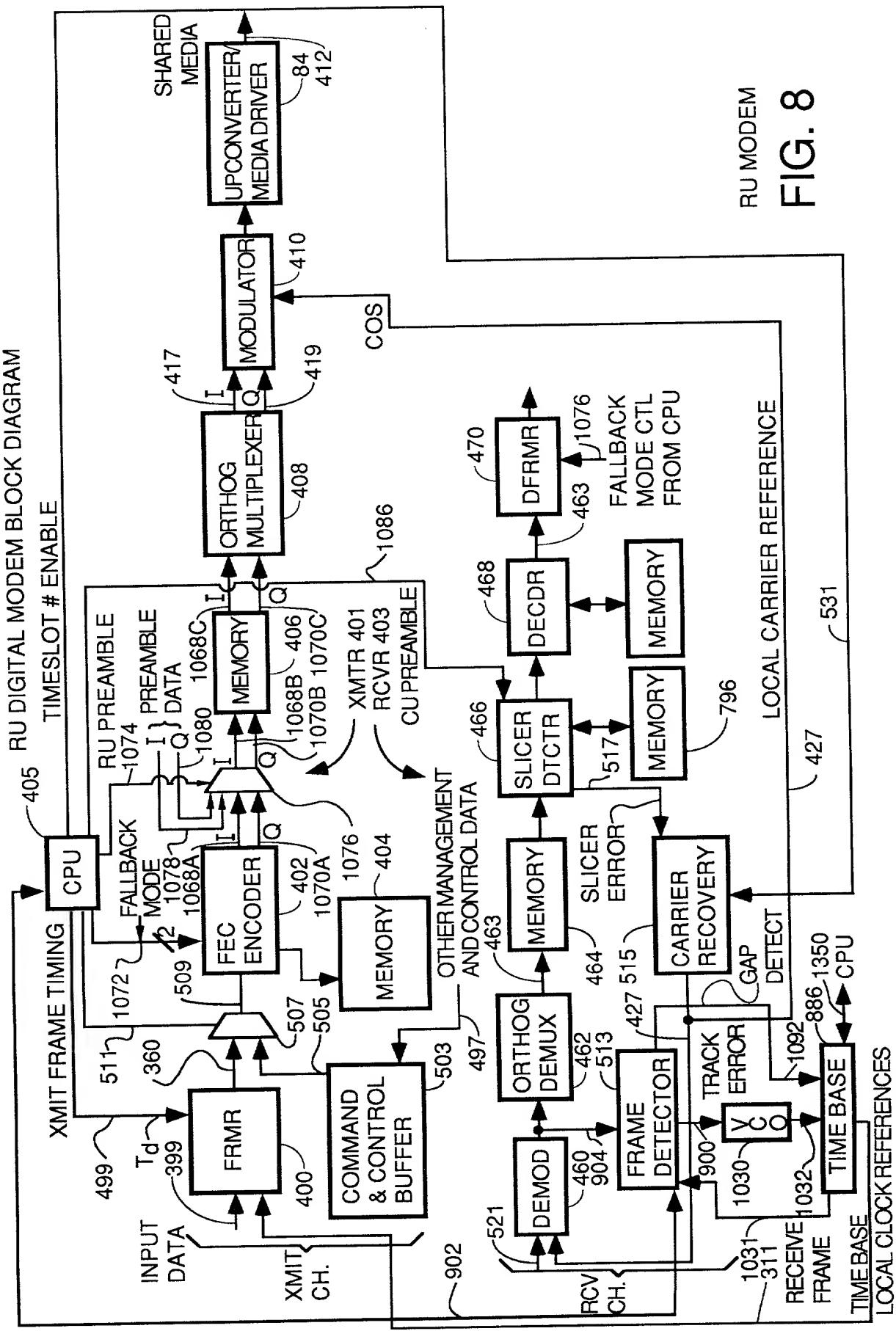


FIG. 8

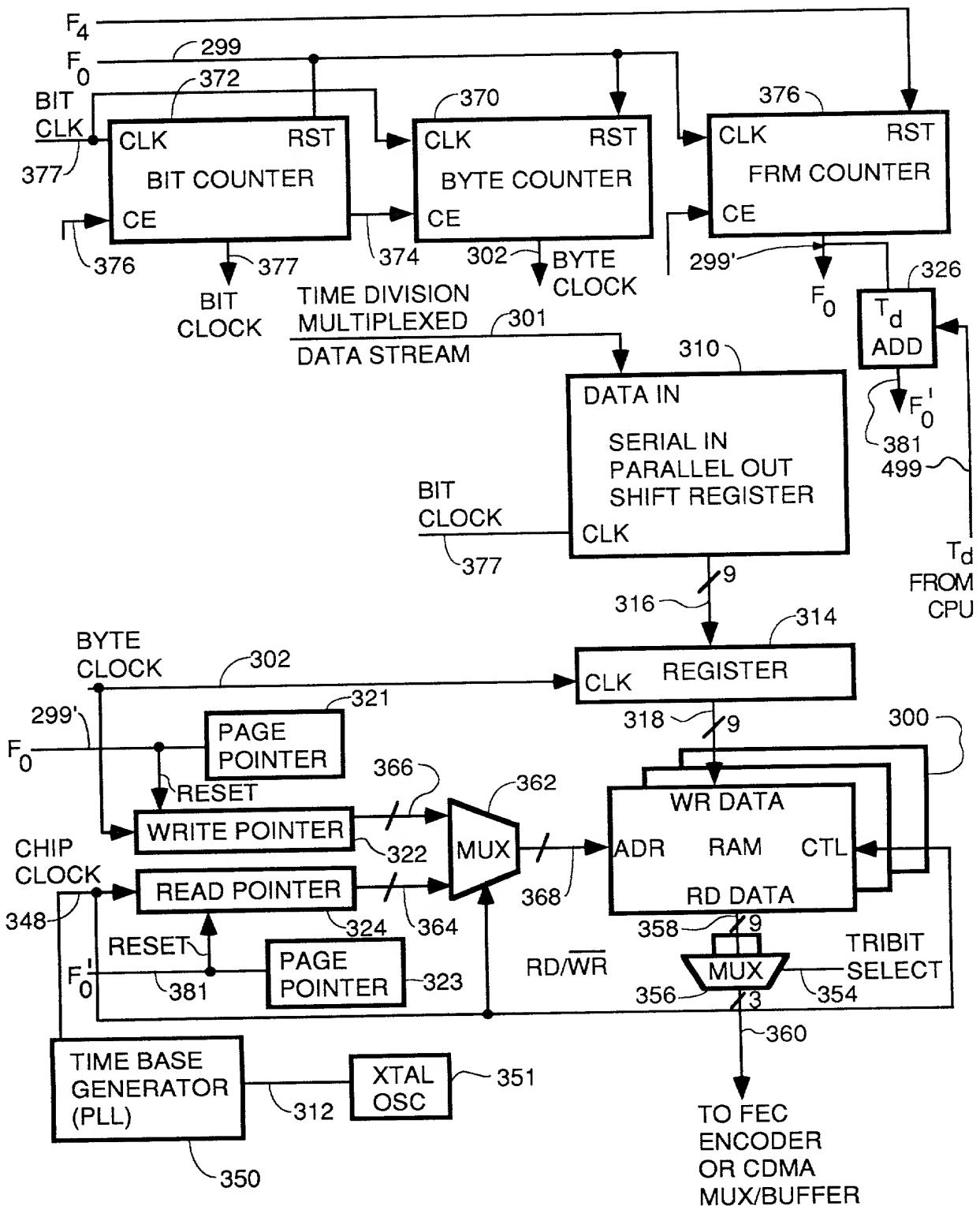


FIG. 9

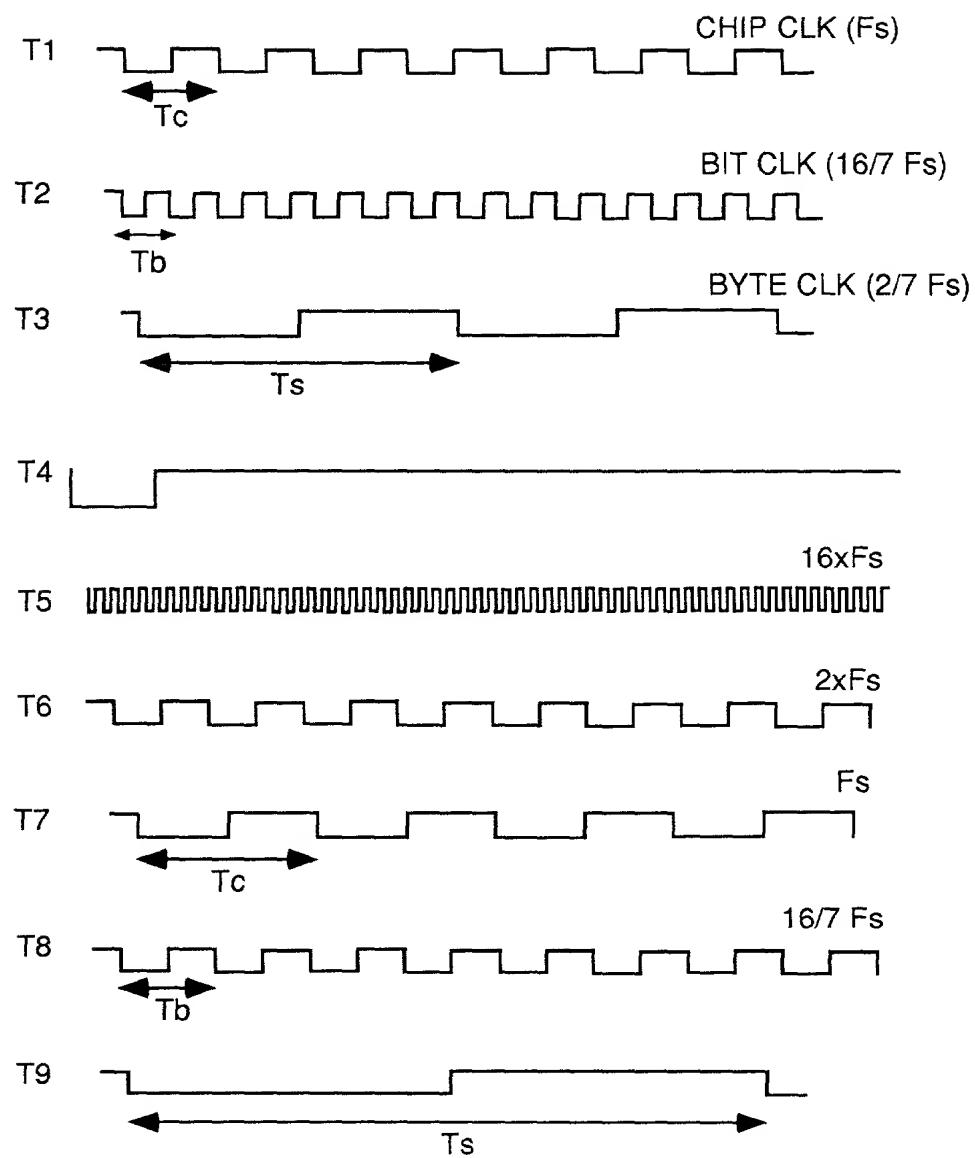


FIG. 10

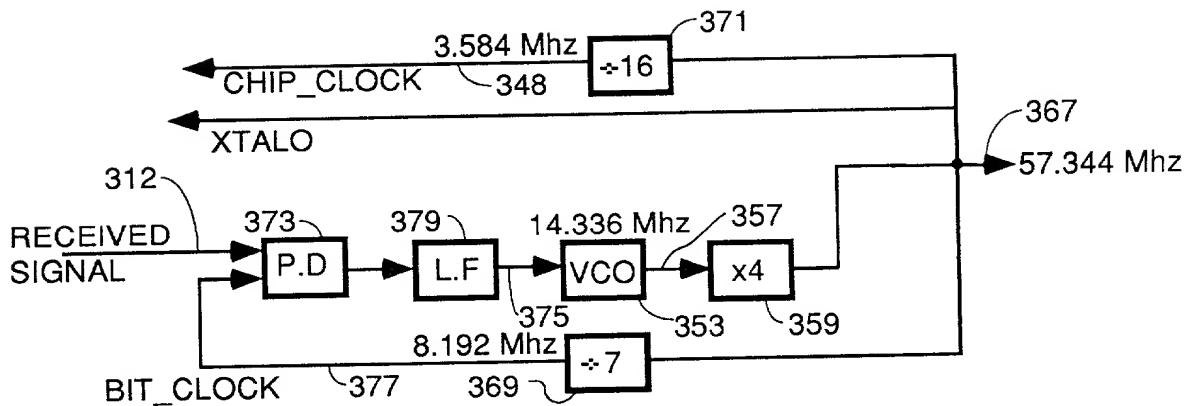


FIG. 11

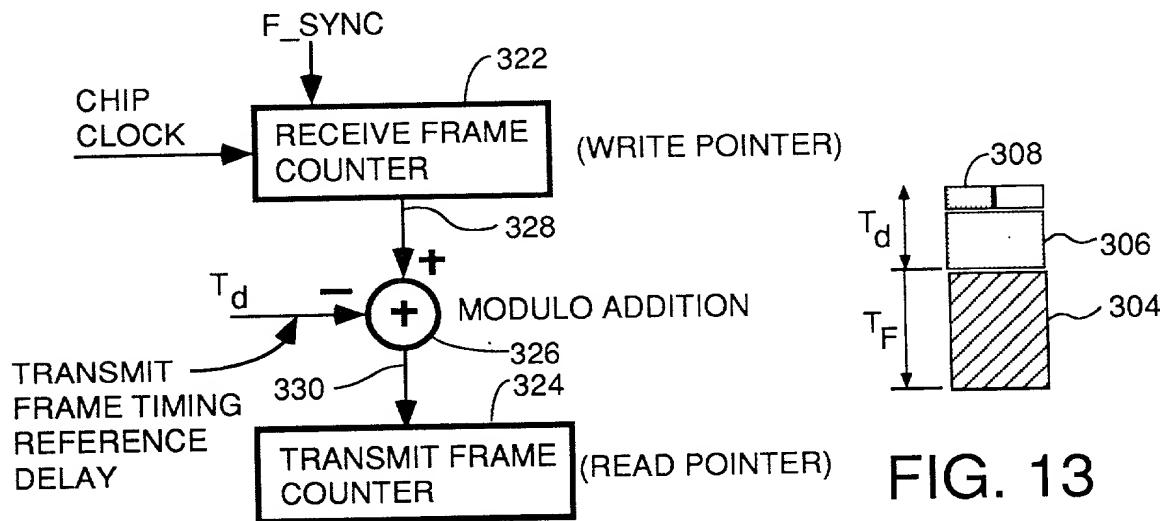


FIG. 12

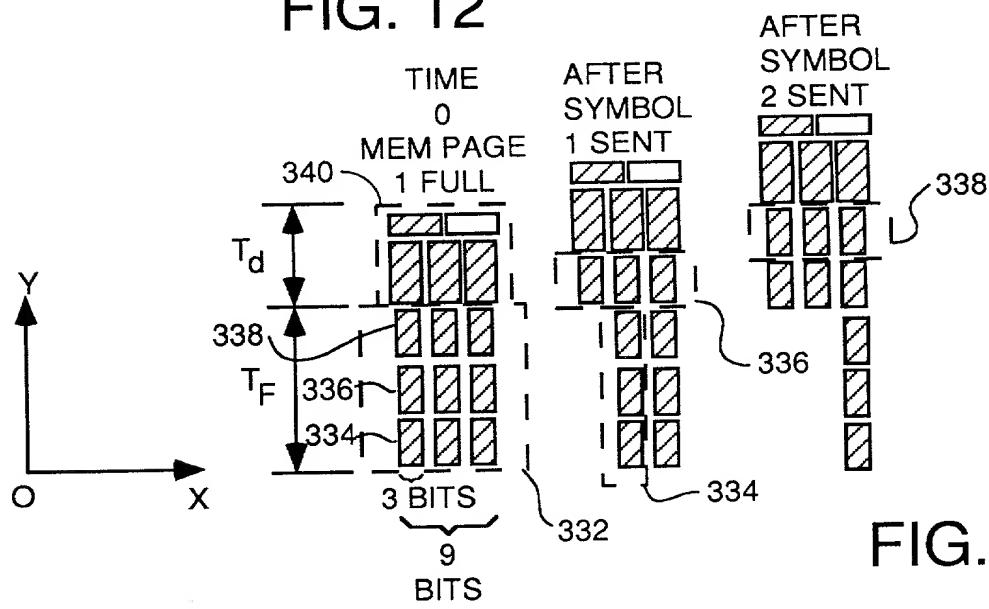


FIG. 14

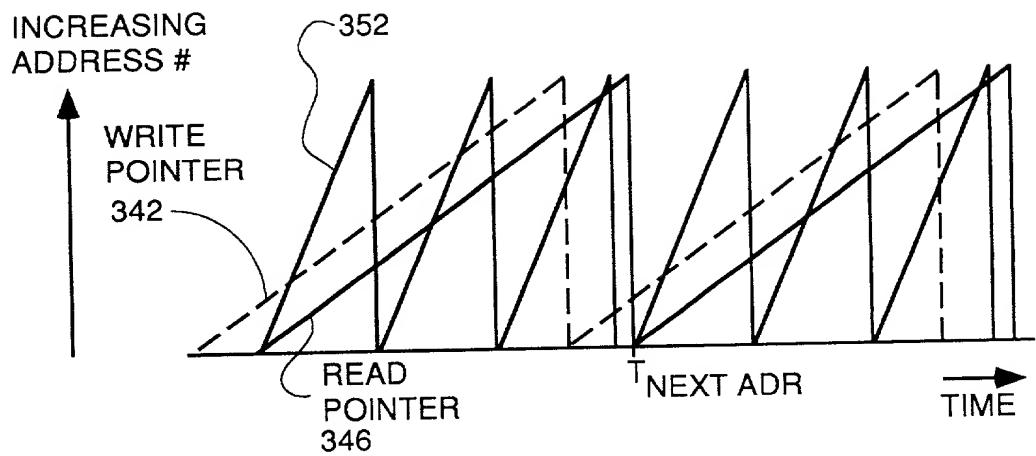


FIG. 15

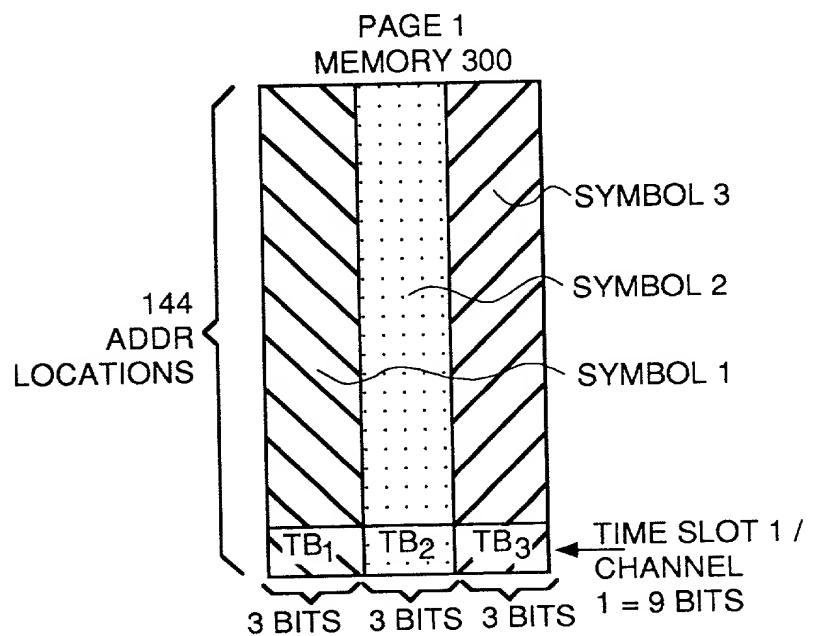
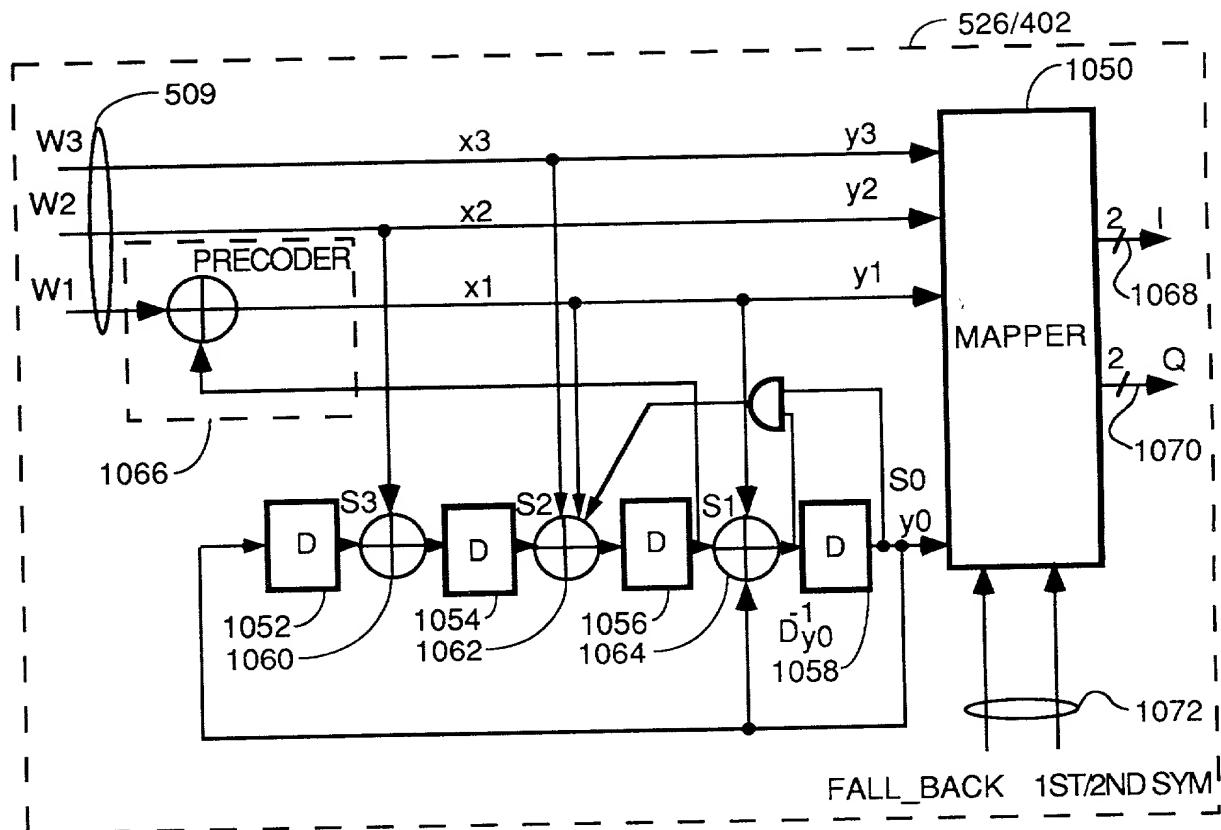


FIG. 16



PREFERRED TRELLIS ENCODER

FIG. 17

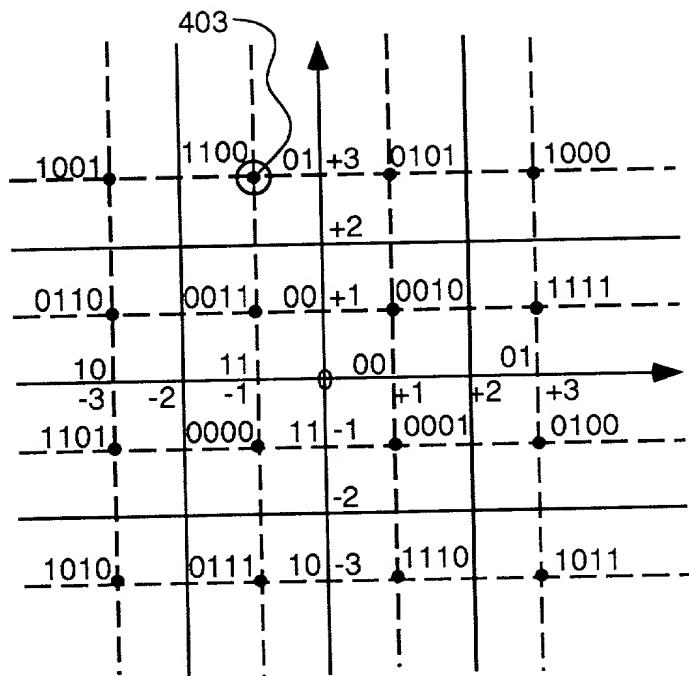


FIG. 18

0000	111	111	
0001	001	111	$= 1 - j$
0010	001	001	$= 1 + j$
0011	111	001	$= -1 + j$
0100	011	111	$= 3 - j$
0101	001	011	$= 1 + 3*j$
0110	101	001	$= -3 + j$
0111	111	101	$= -1 - 3*j$
1000	011	011	$= +3 + 3*j$
1001	101	011	$= -3 + 3*j$
1010	101	101	$= -3 - 3*j$
1011	011	101	$= 3 - 3*j$
1100	111	011	$= -1 + 3*j$
1101	101	111	$= -3 - j$
1110	001	101	$= 1 - 3*j$
1111	011	001	$= 3 + j$

FIG. 19

INFORMATION
VECTOR [B]
FOR EACH
SYMBOL

$$\begin{bmatrix} 0110 \\ 1111 \\ 1101 \\ 0100 \\ \vdots \end{bmatrix}$$

ORTHOGONAL
CODE MATRIX

$$x \begin{bmatrix} c_{1,1} & c_{1,2} & \cdots & c_{1,144} \\ c_{2,1} & c_{2,2} & \cdots & c_{2,144} \\ \vdots & \vdots & & \vdots \end{bmatrix}$$

FIG. 20A

REAL PART OF INFO VECTOR [b] FOR FIRST SYMBOL

REAL PART OF RESULT VECTOR

$$405 \begin{bmatrix} +3 \\ -1 \\ -1 \\ +3 \end{bmatrix} \cdot \begin{bmatrix} 1 & 1 & 1 & 1 \\ -1 & -1 & 1 & 1 \\ -1 & 1 & -1 & 1 \\ -1 & 1 & 1 & -1 \end{bmatrix} = \begin{bmatrix} 4 \\ 0 \\ 0 \\ -8 \end{bmatrix} \quad 409$$

$[b_{\text{REAL}}] \times [\text{CODE MATRIX}] = [R_{\text{REAL}}] = \text{"CHIPS OUT" ARRAY-REAL}$

FIG. 20B

MAPPING FOR FALL-BACK MODE - LSB'S

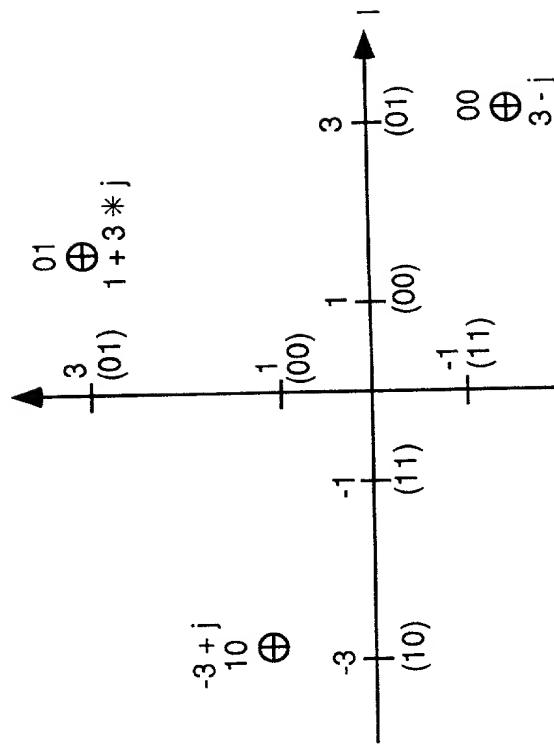


FIG. 21

MSBs $y_3 \ y_2$	PHASE difference (2nd-1st symbol)	$1+jQ$ WHEN $LSB=00$	$1+jQ$ WHEN $LSB=01$	$1+jQ$ WHEN $LSB=10$	$1+jQ$ WHEN $LSB=11$
00	0	$3-j$	$1+j3$	$-3+j$	$-1-j3$
01	90	$1+j3$	$-3+j$	$-1-j3$	$3-j$
10	180	$-3+j$	$-1-j3$	$3-j$	$1+j3$
11	-90	$-1-j3$	$3-j$	$1+j3$	$-3+j$

LSB & MSB FALLBACK MODE MAPPINGS

FIG. 22

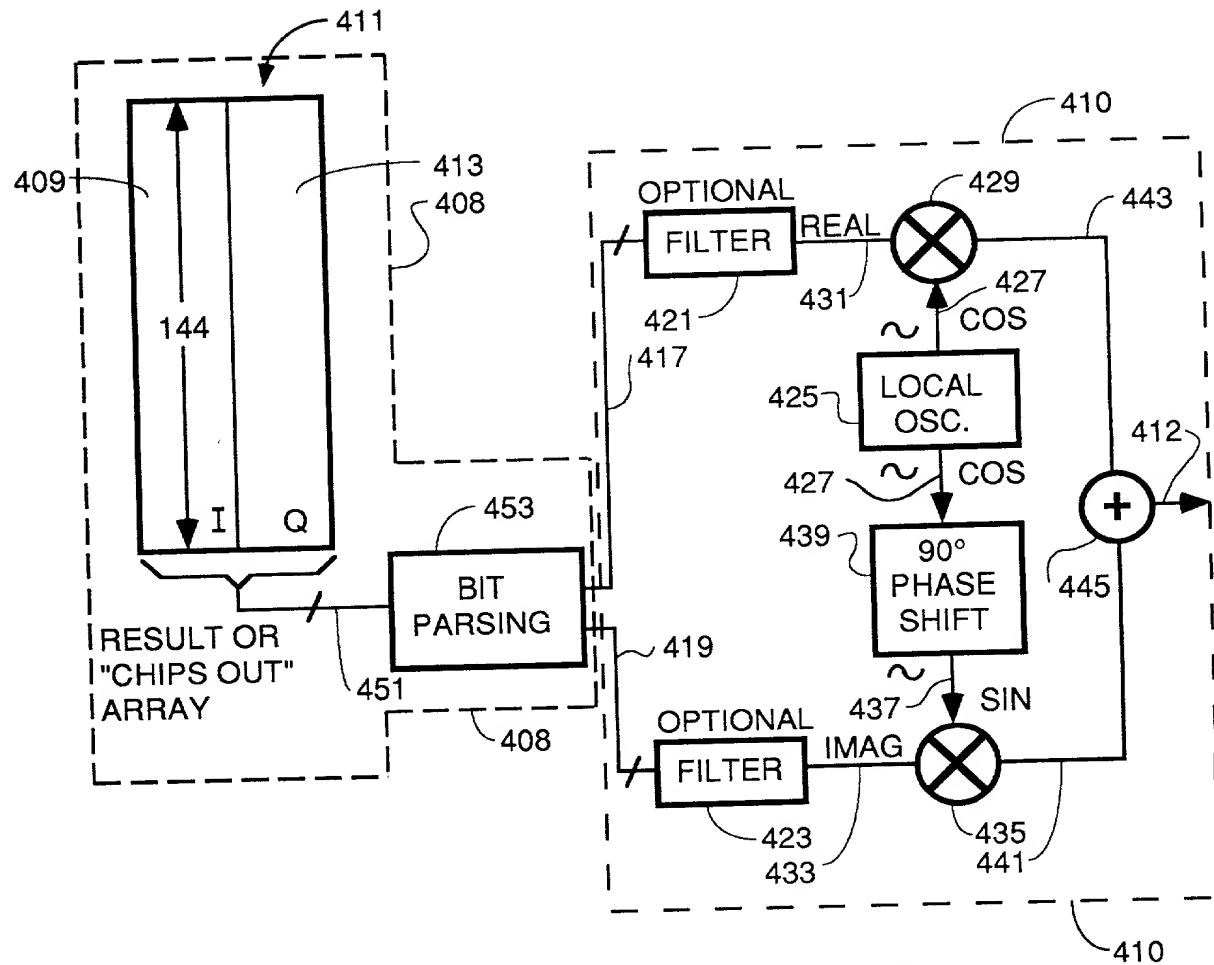


FIG. 23

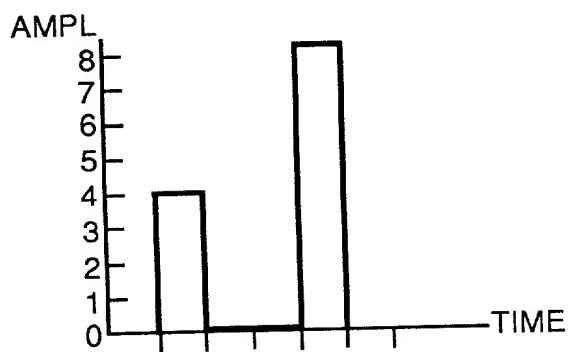


FIG. 24

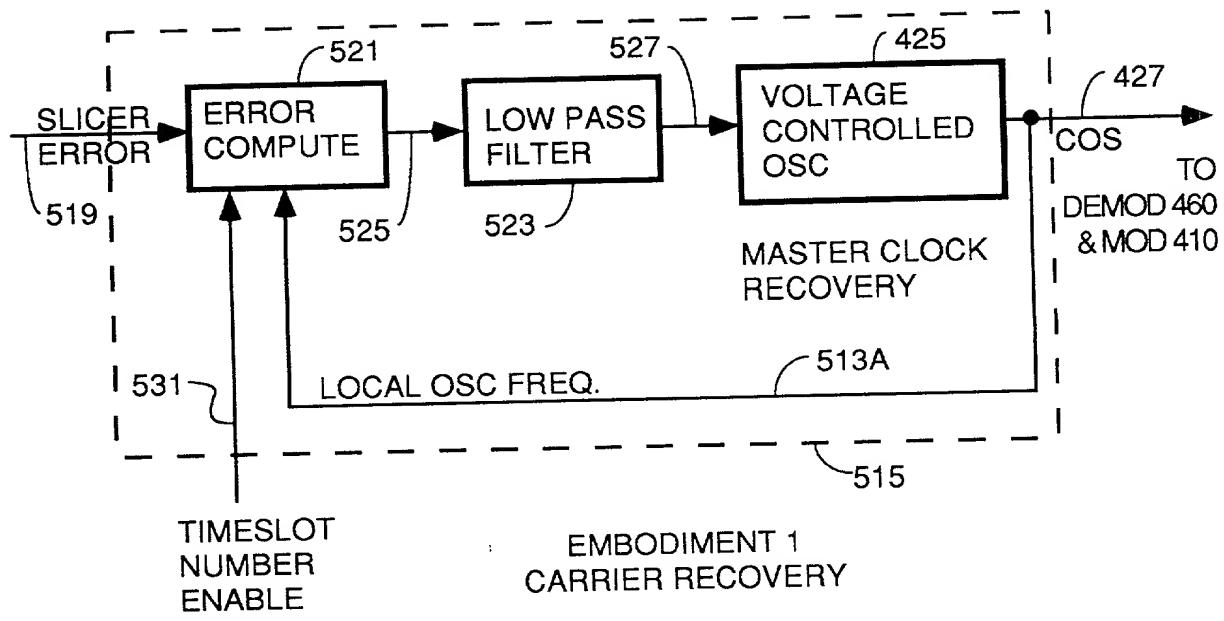


FIG. 25

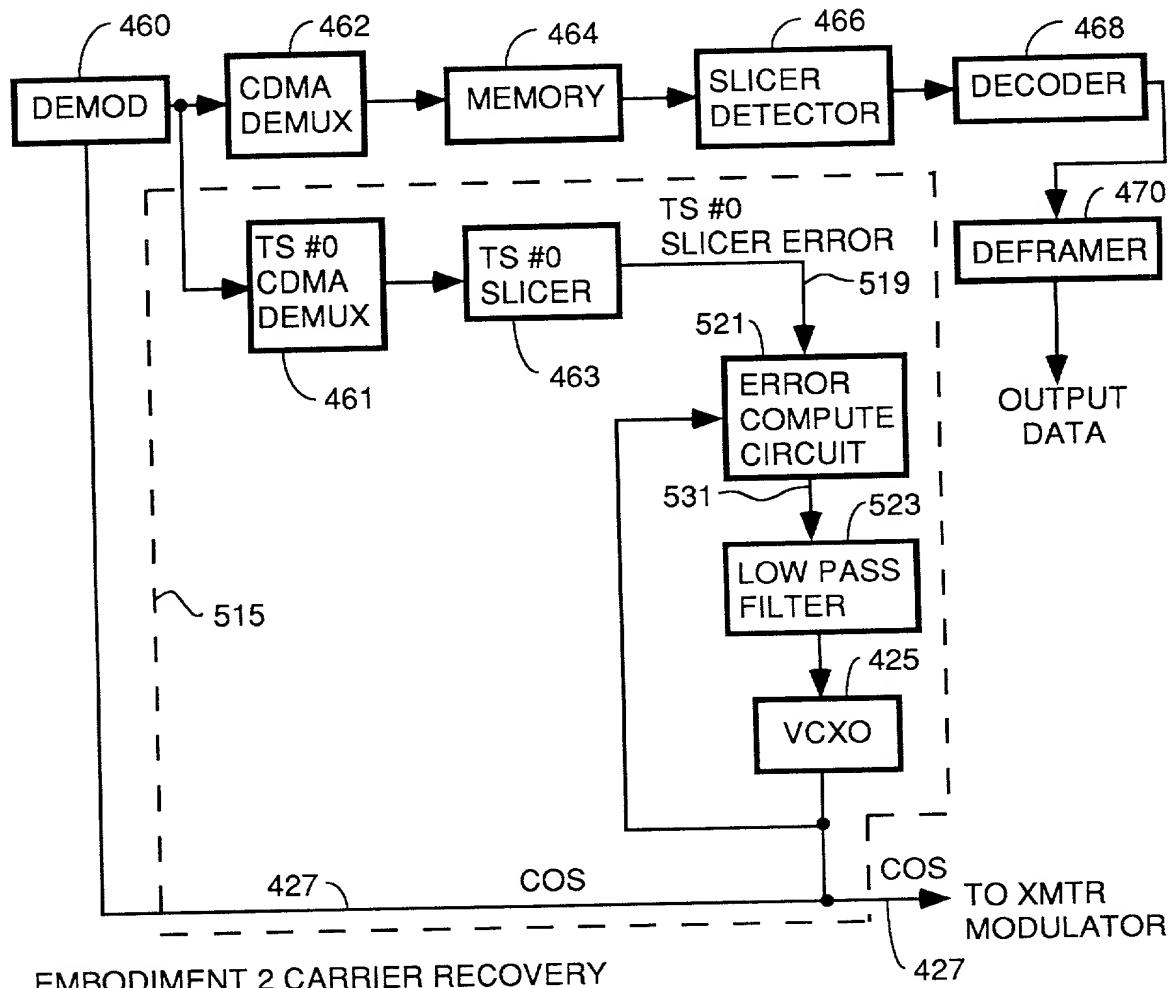


FIG. 26

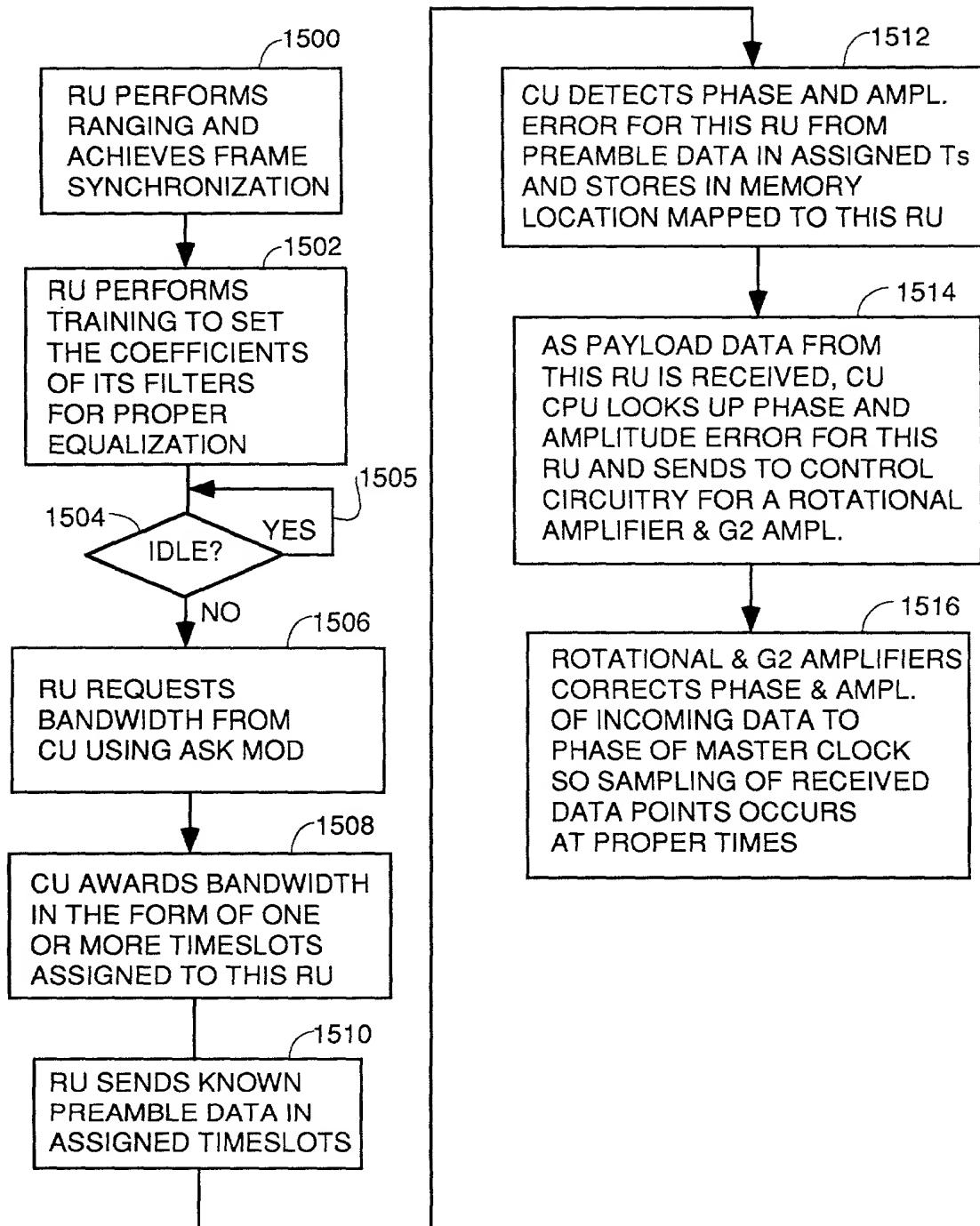
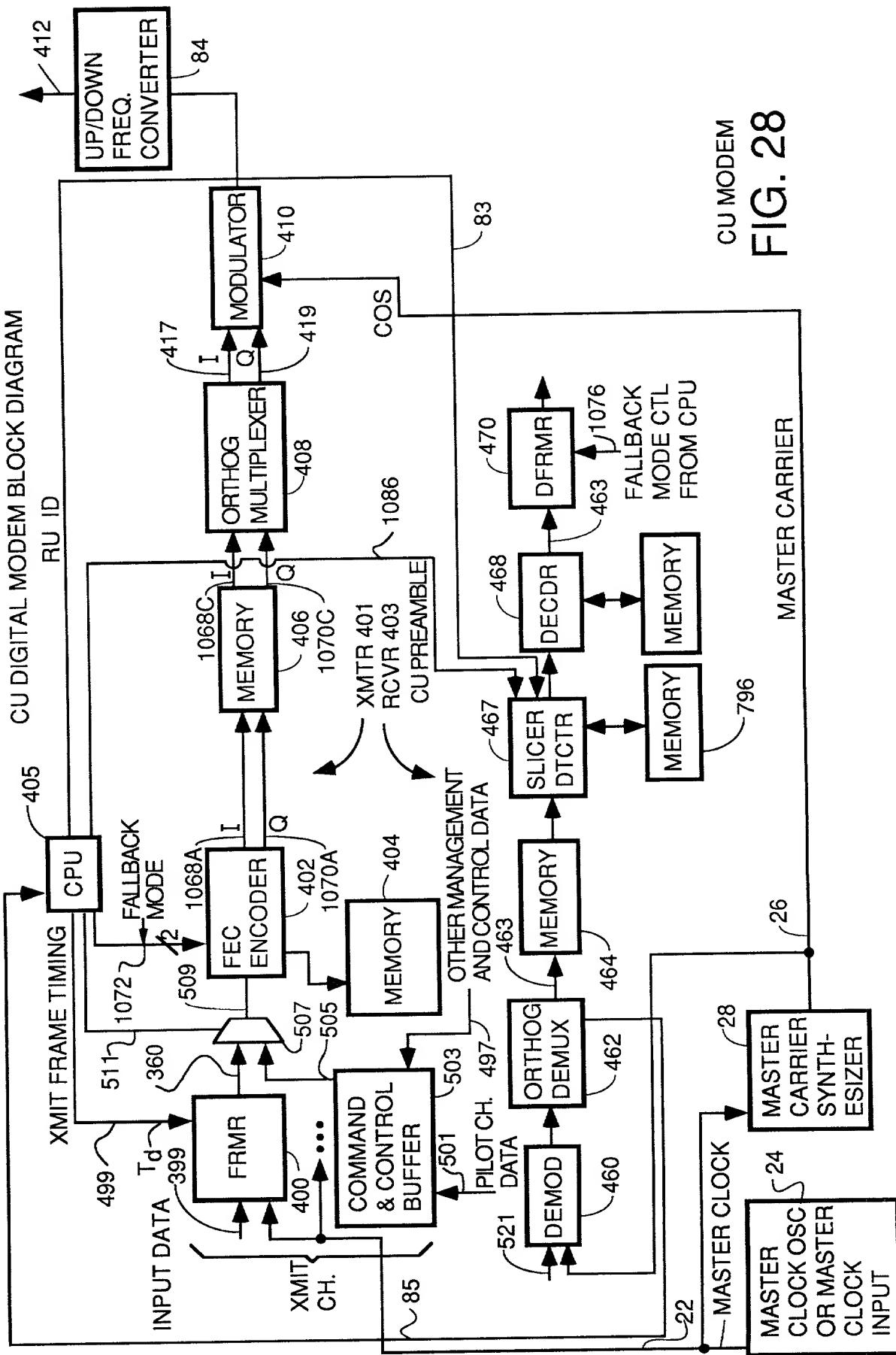


FIG. 27

FIG. 28



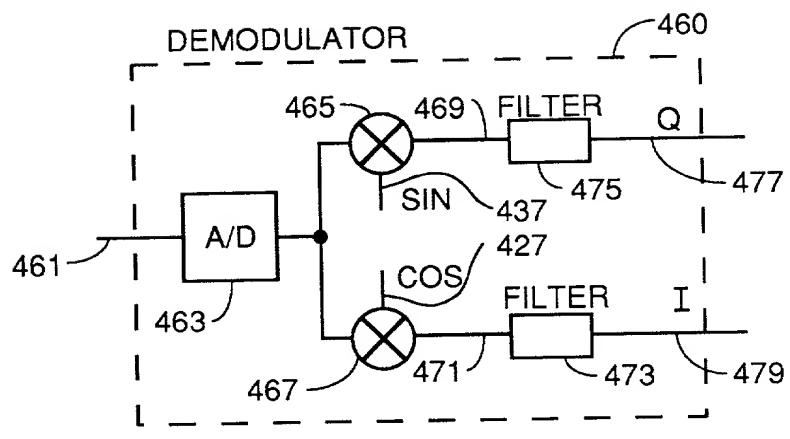


FIG. 29

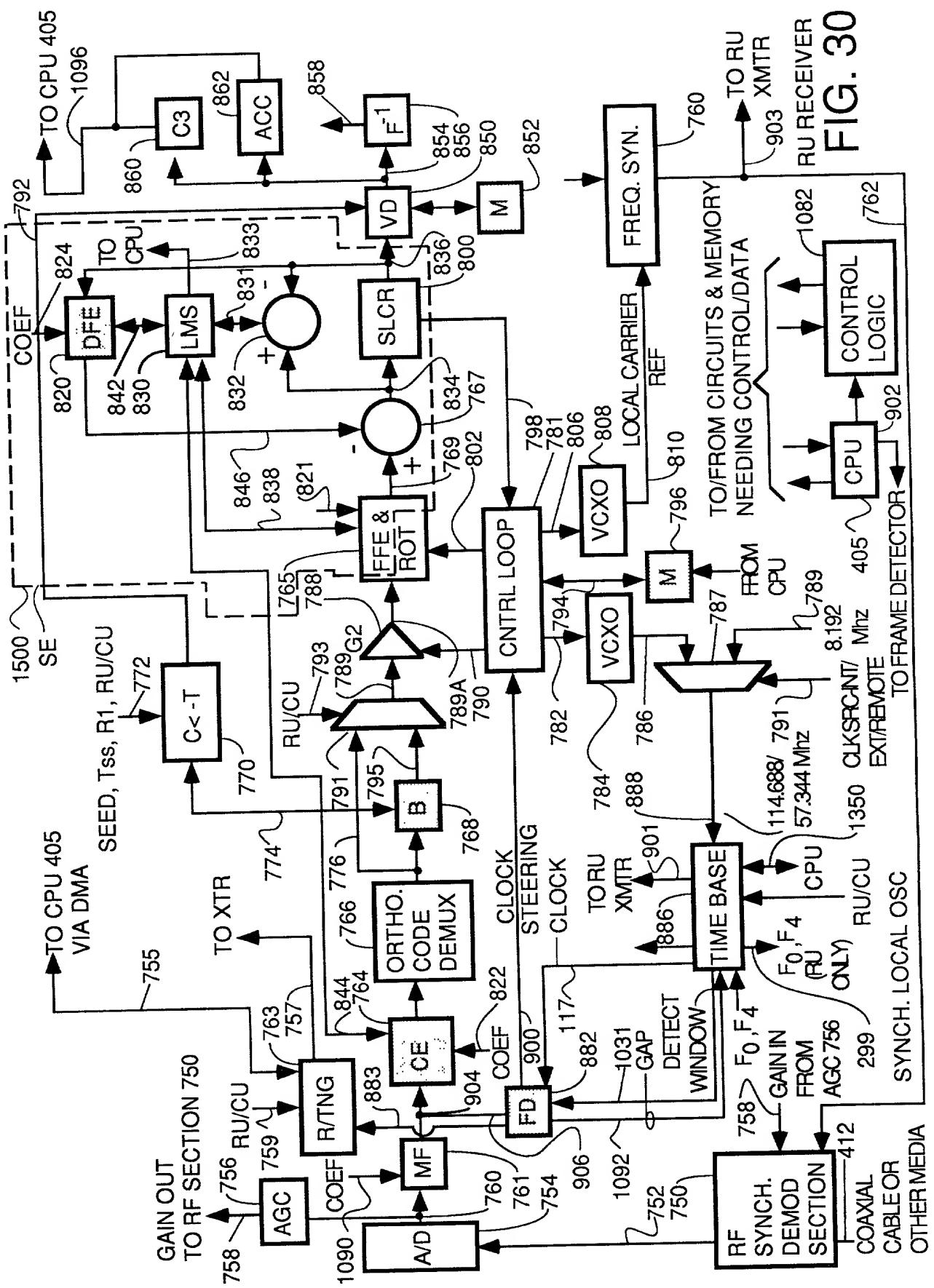
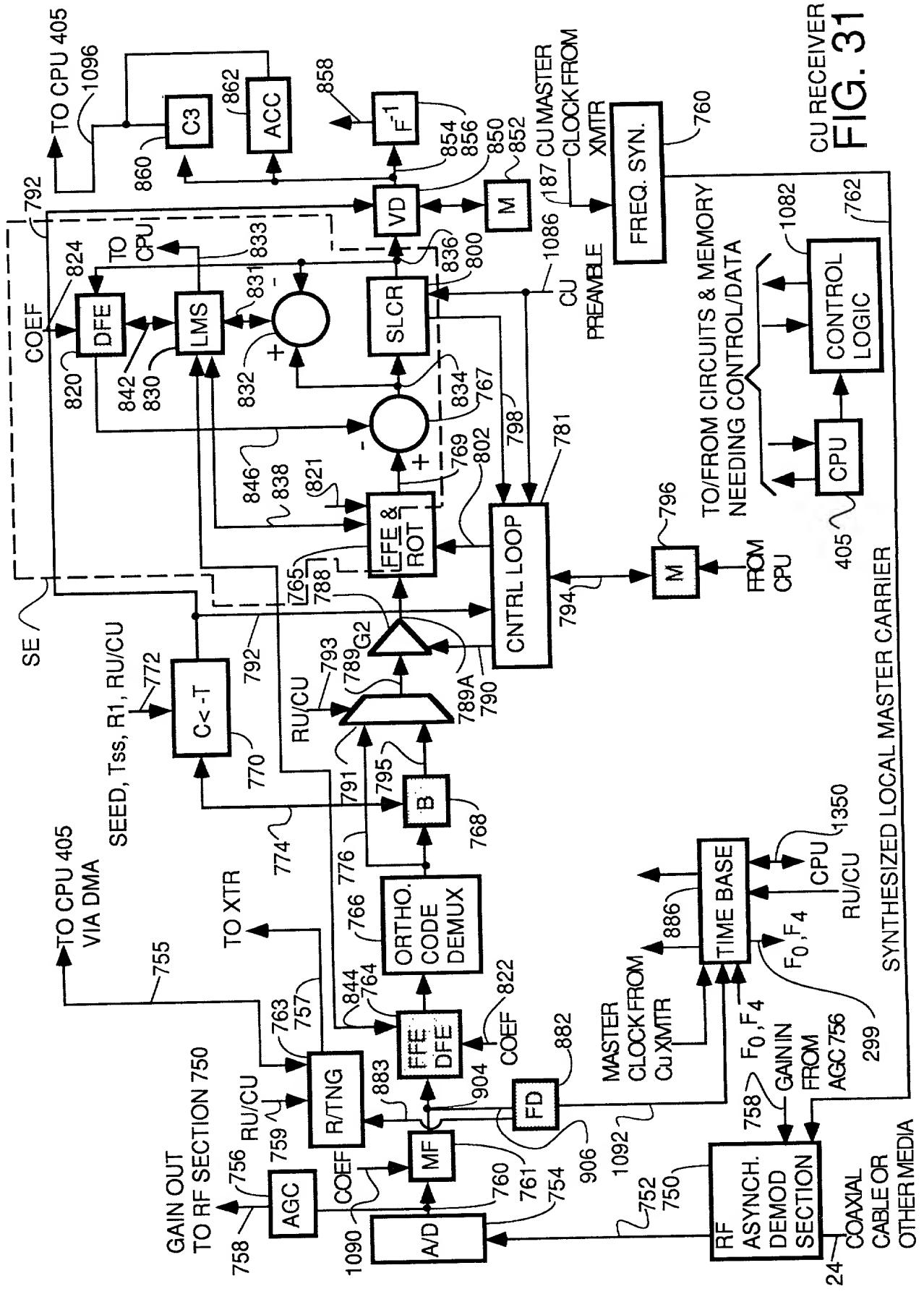
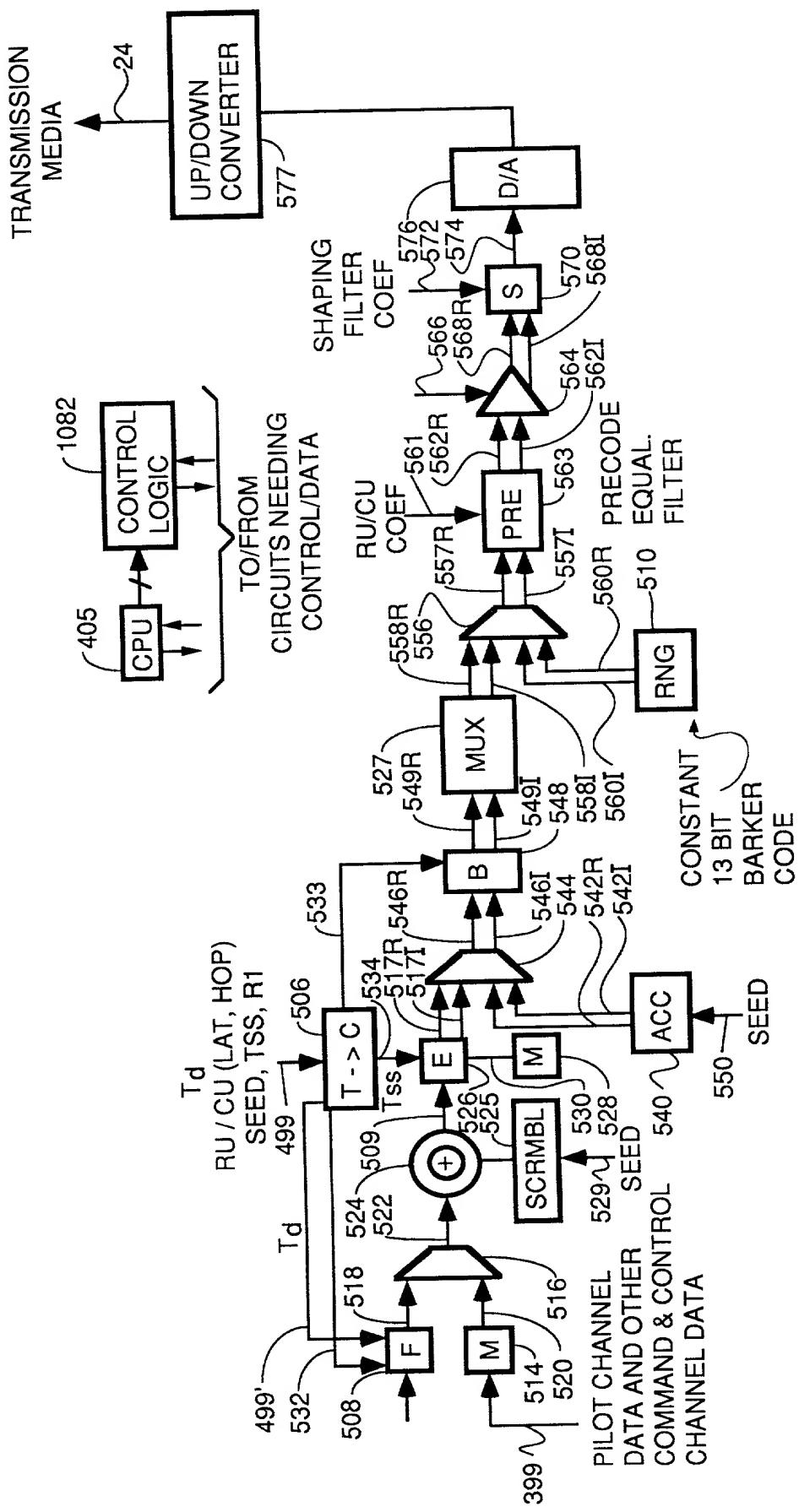


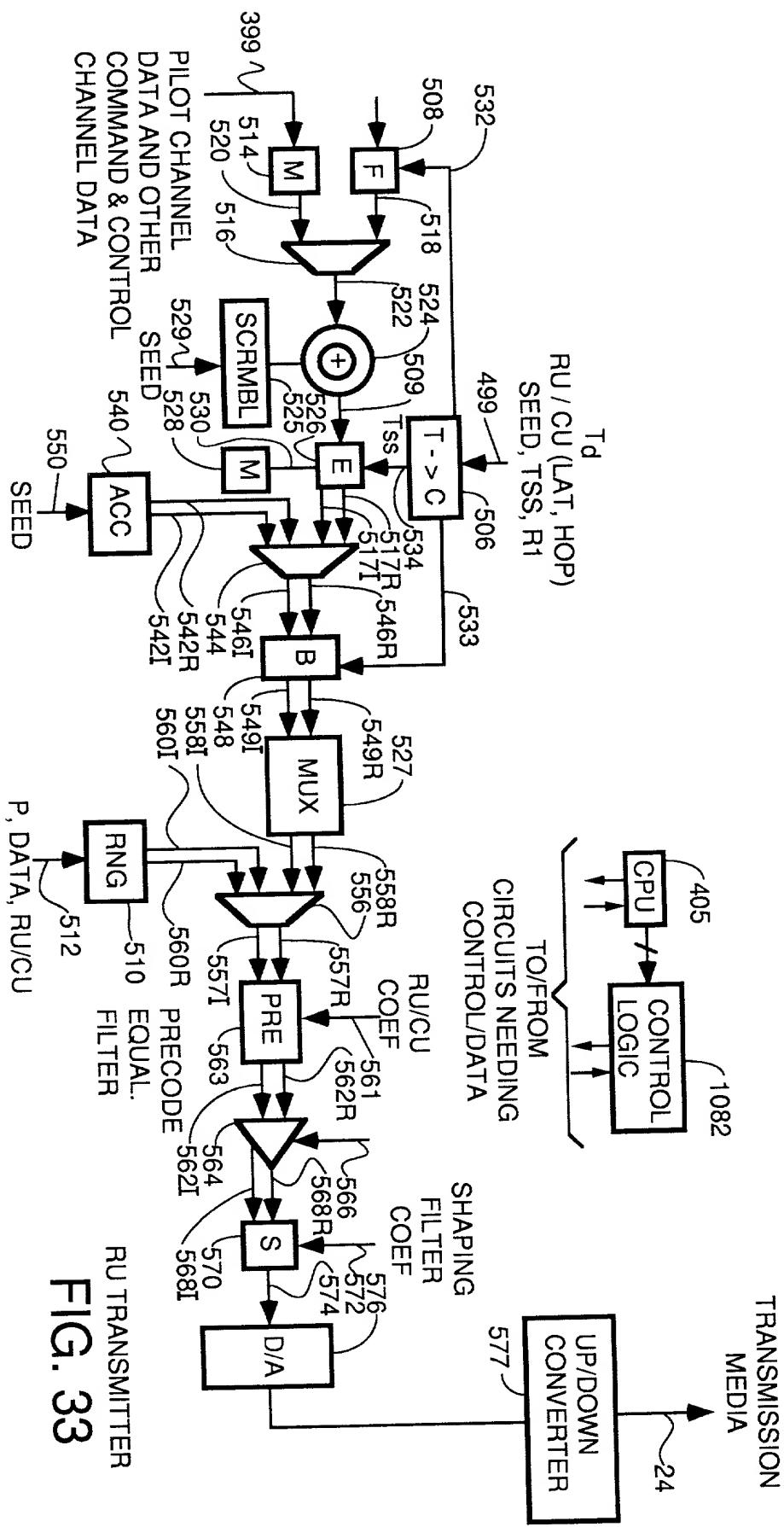
FIG. 30

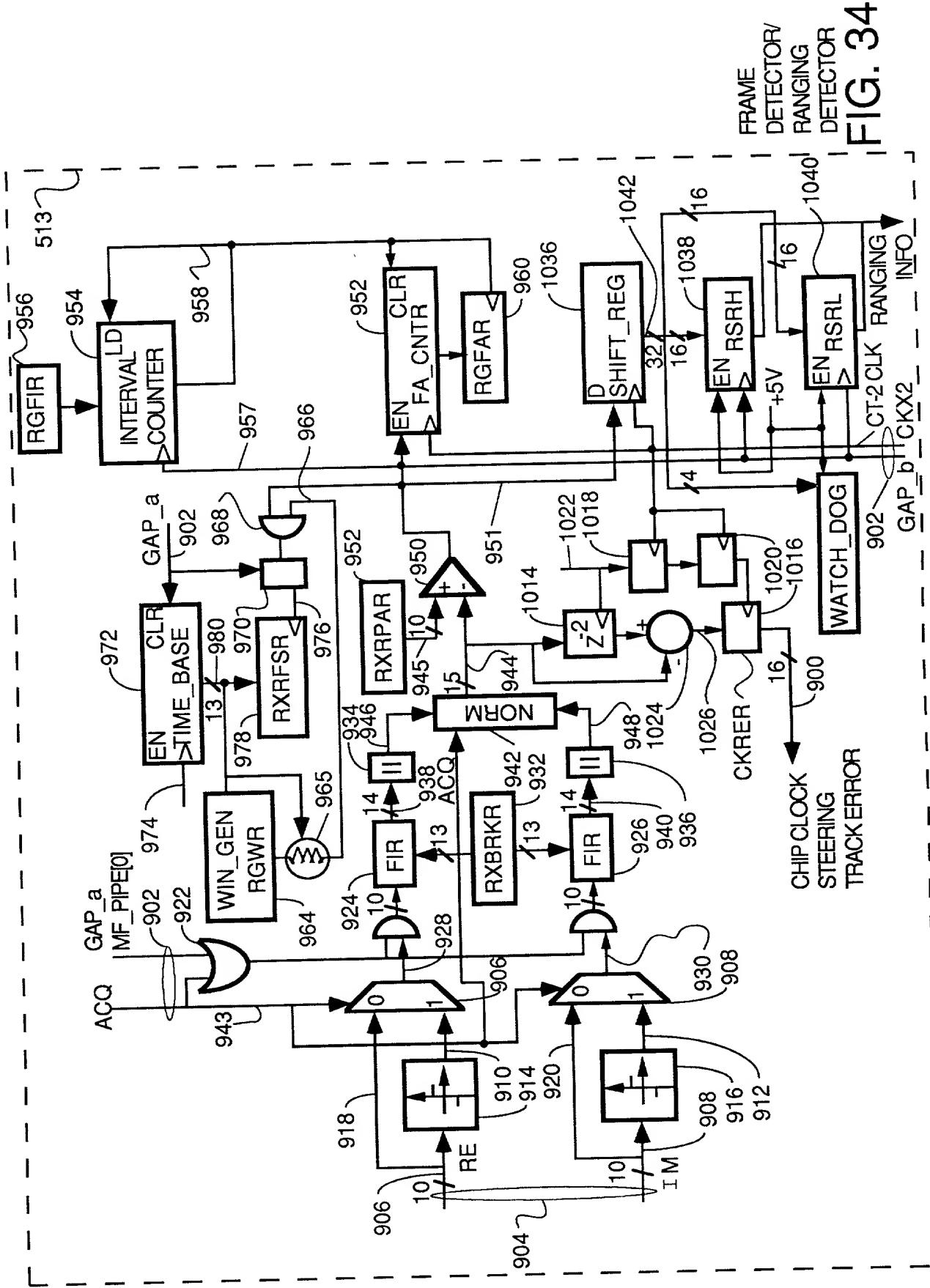


CU RECEIVER
FIG. 31

FIG. 32







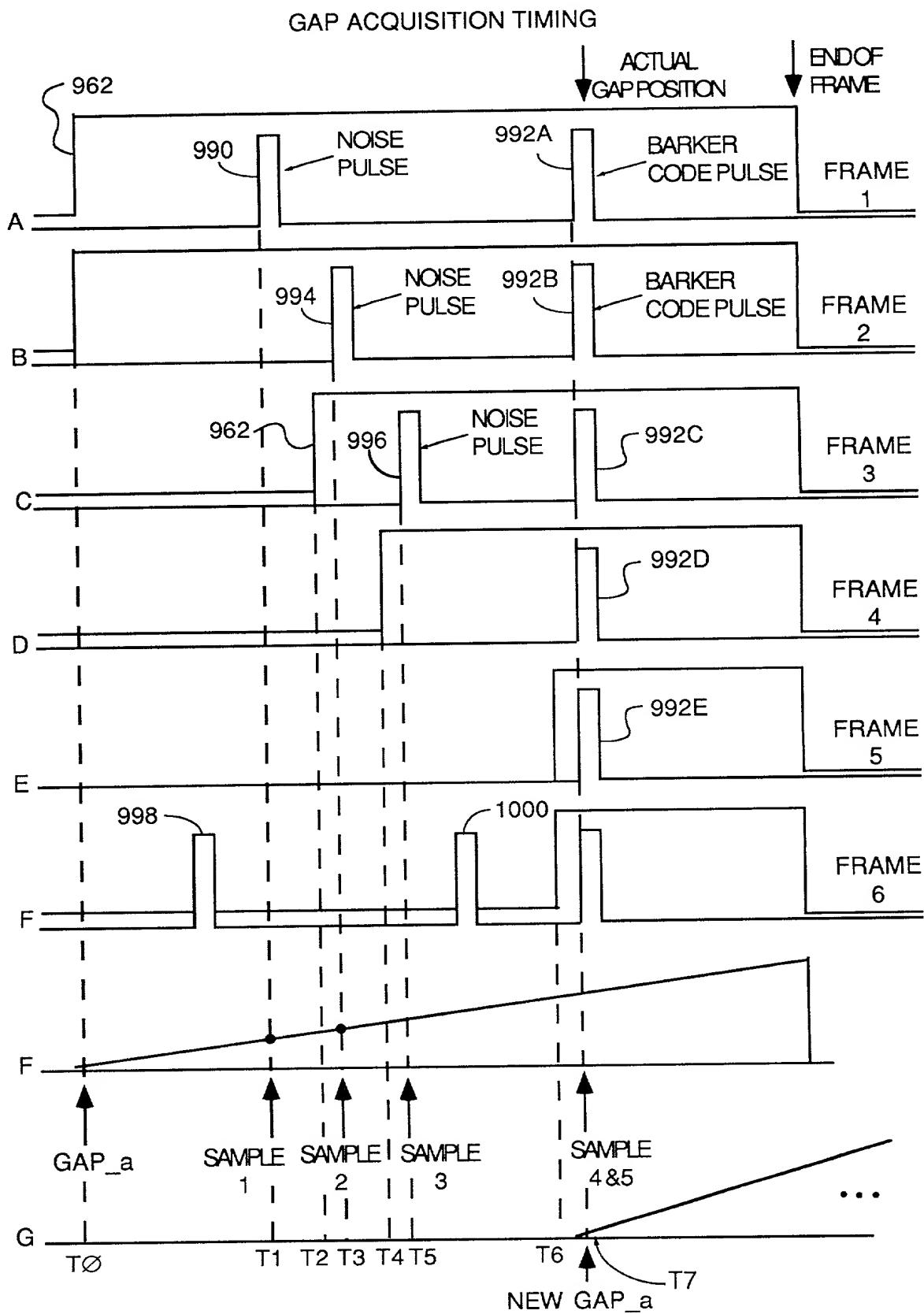


FIG. 35

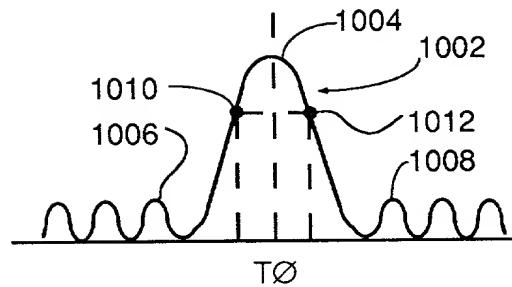


FIG. 36

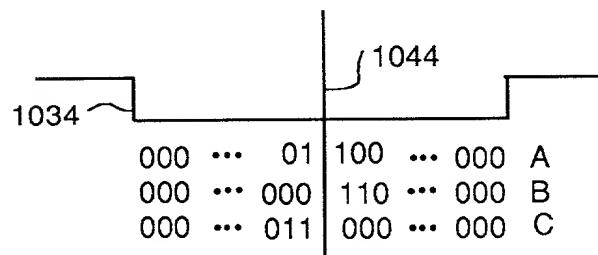


FIG. 37
FINE TUNING TO
CENTER BARKER CODE

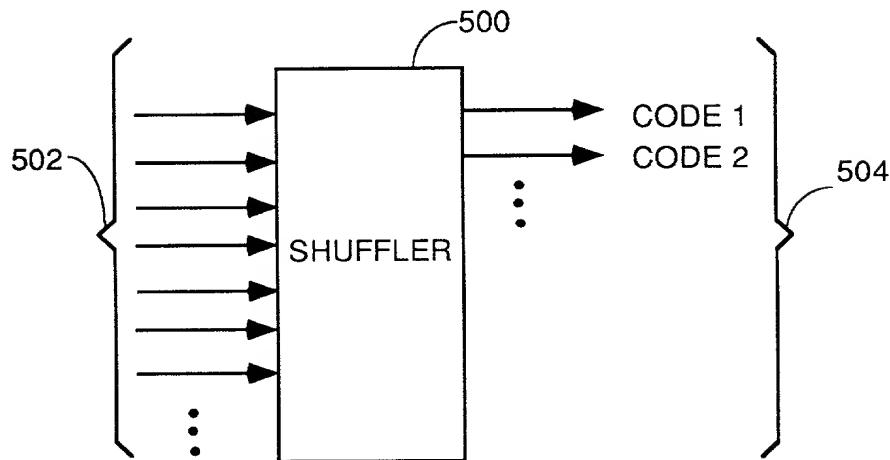
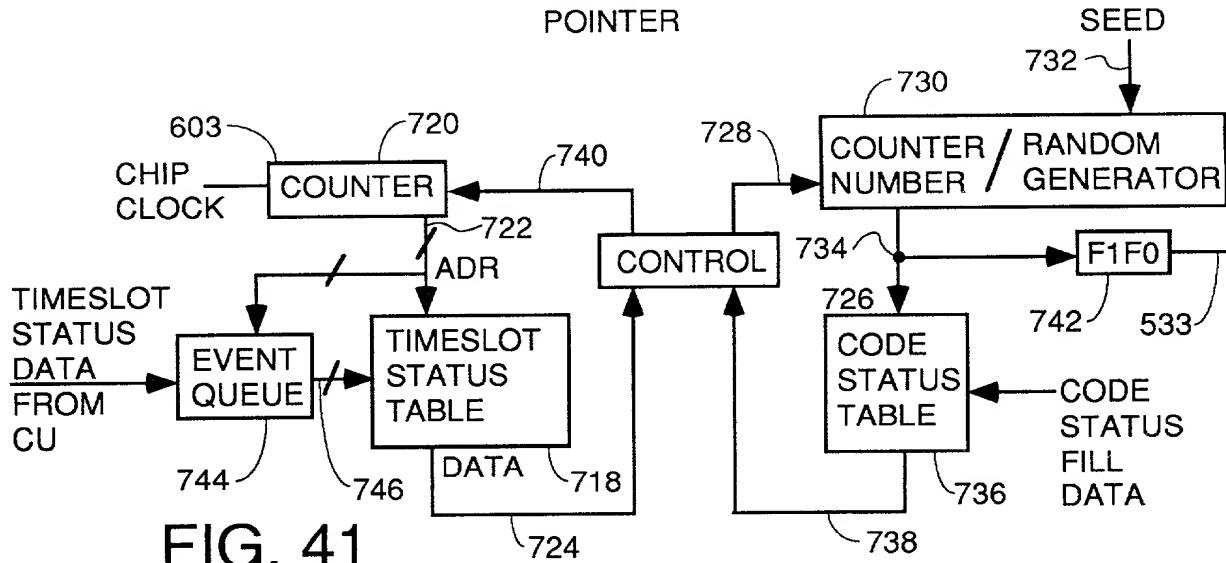
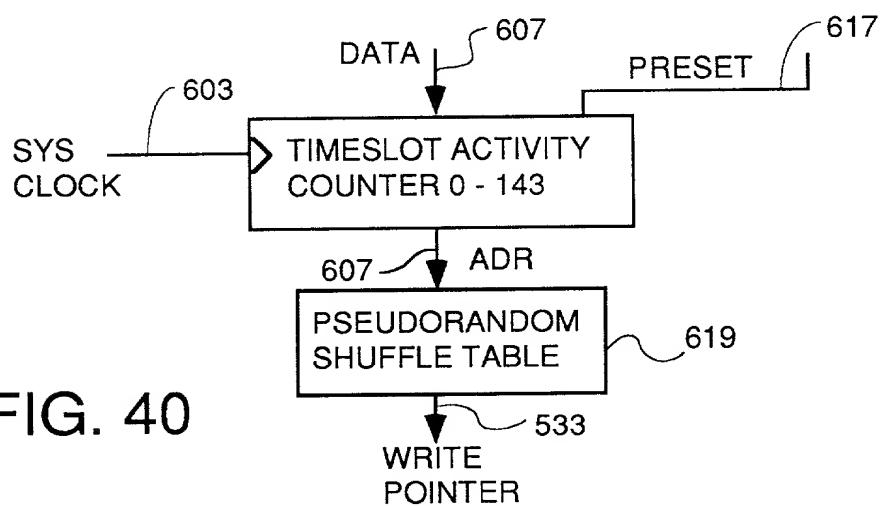
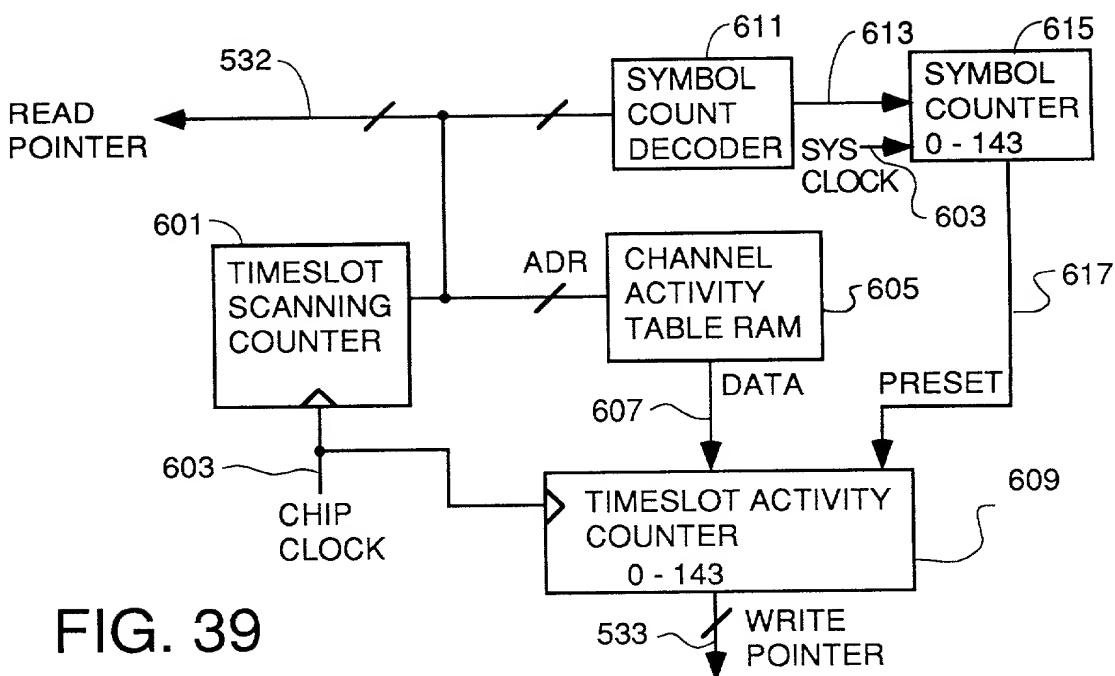


FIG. 38



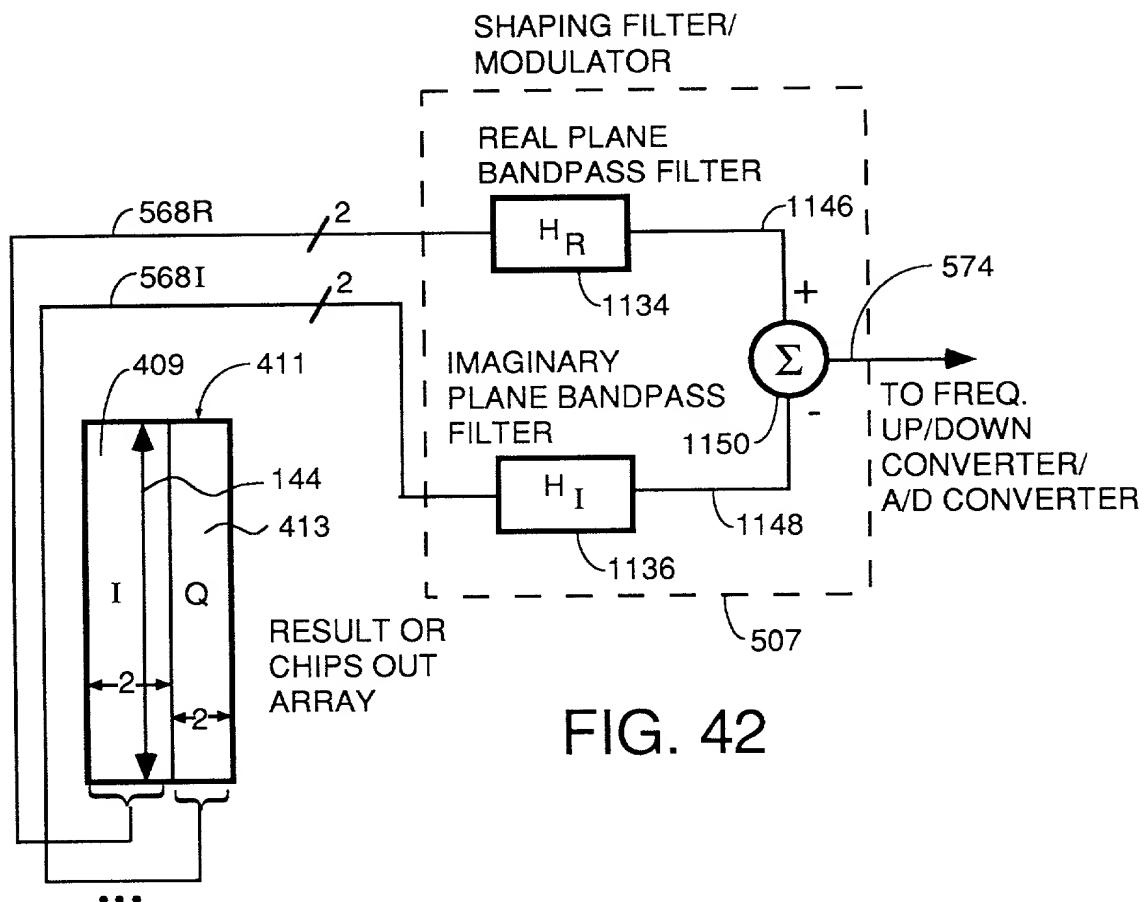


FIG. 42

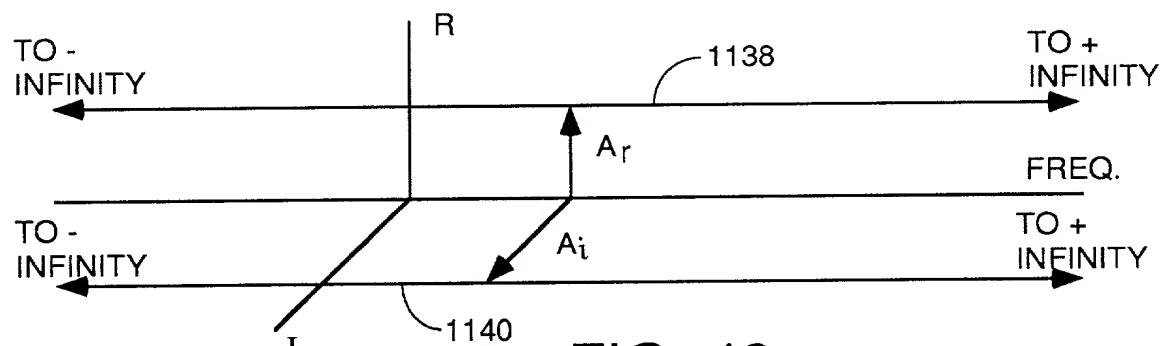


FIG. 43

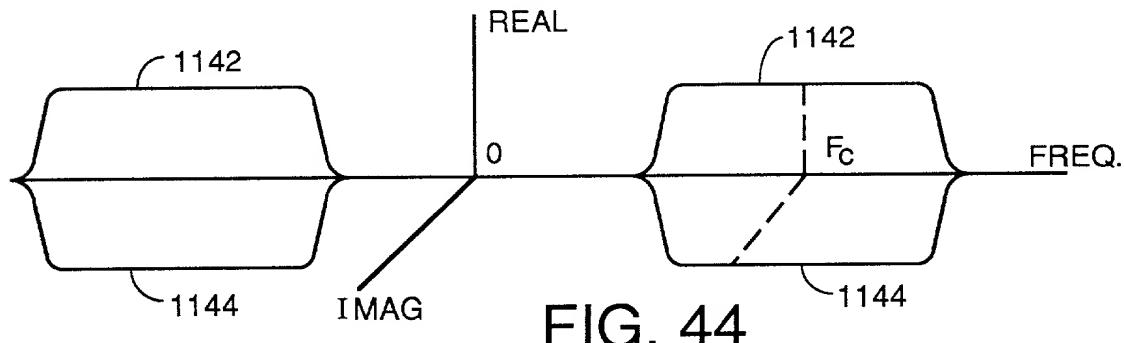
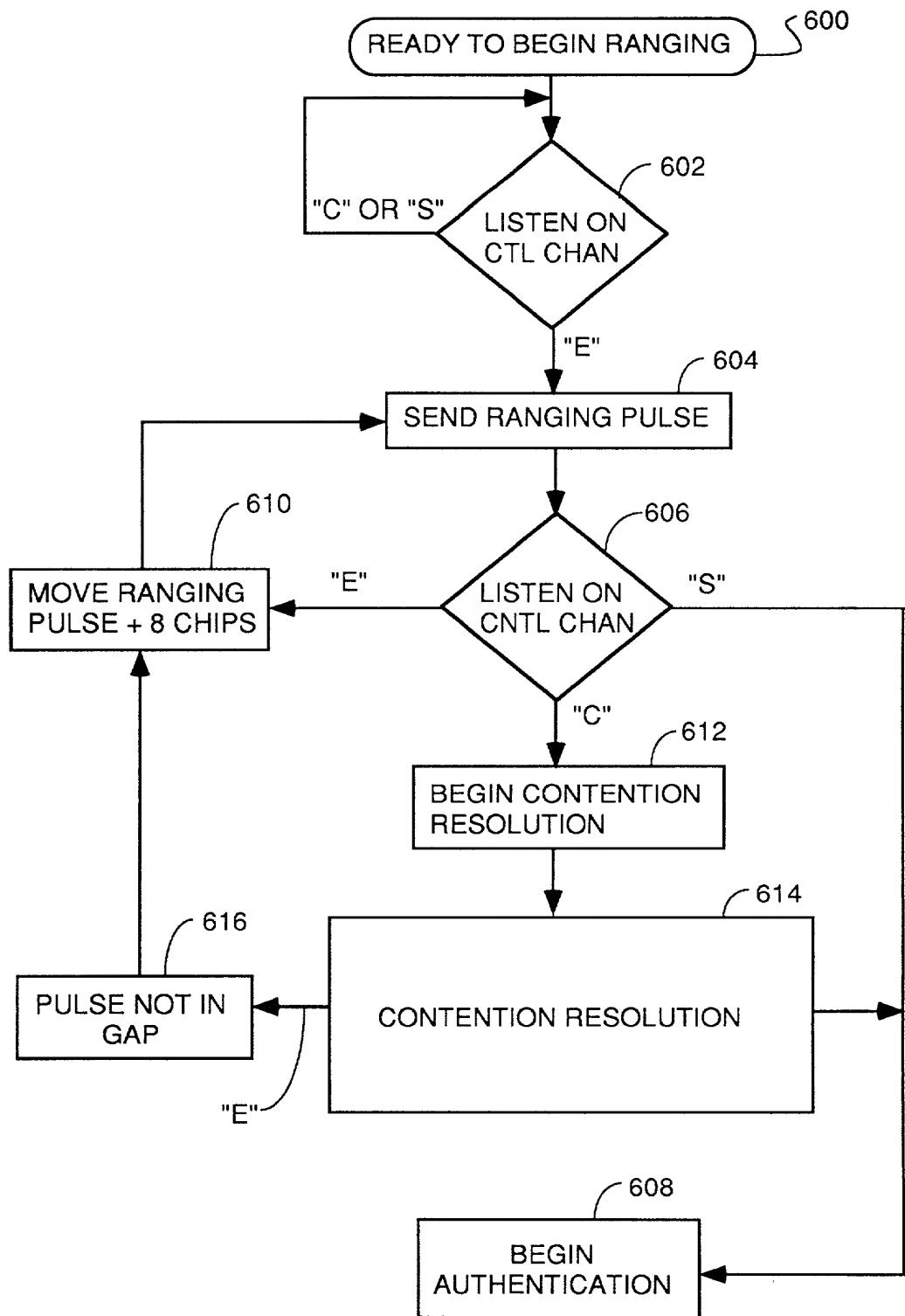
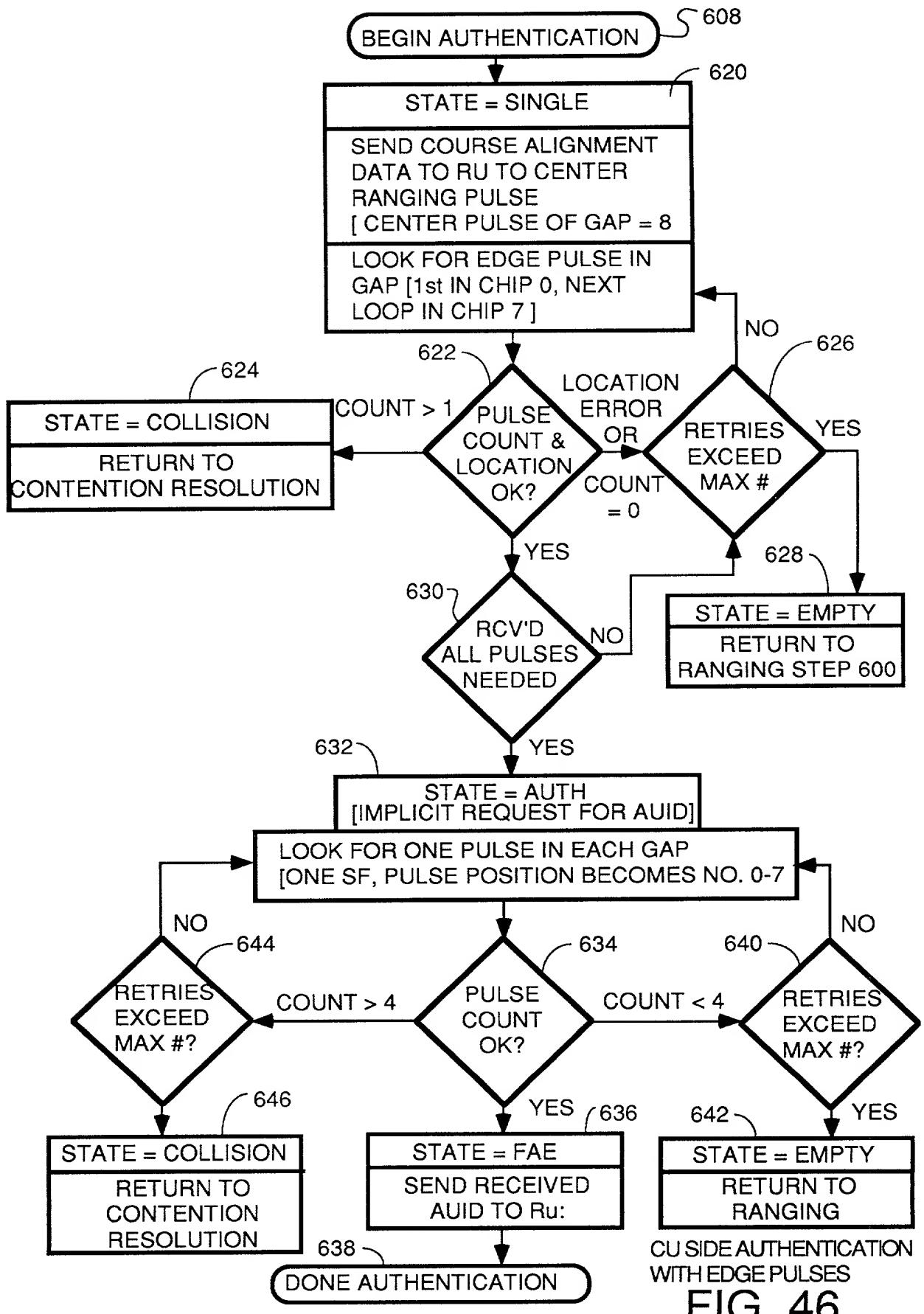


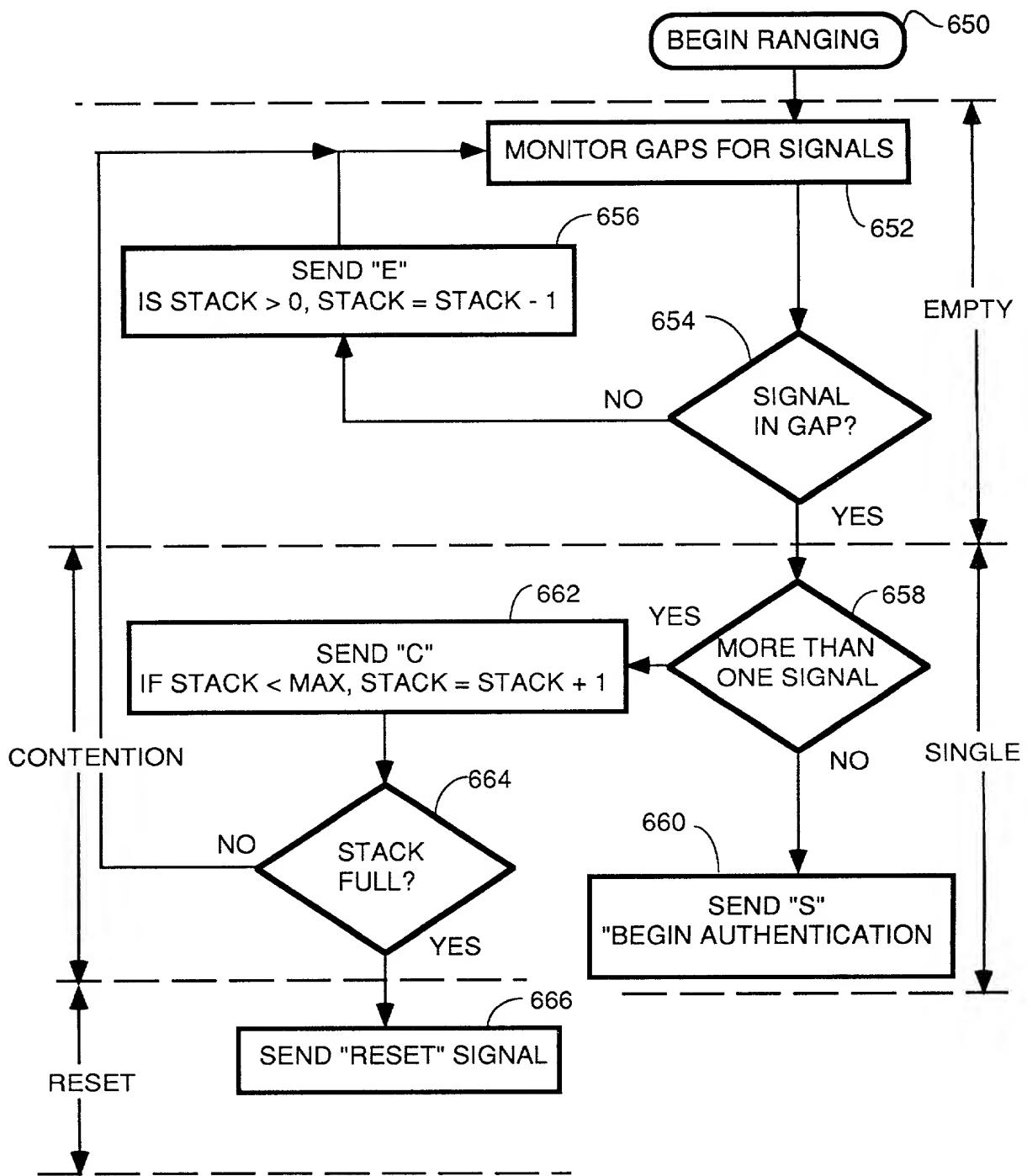
FIG. 44



RU RANGING
FIG. 45

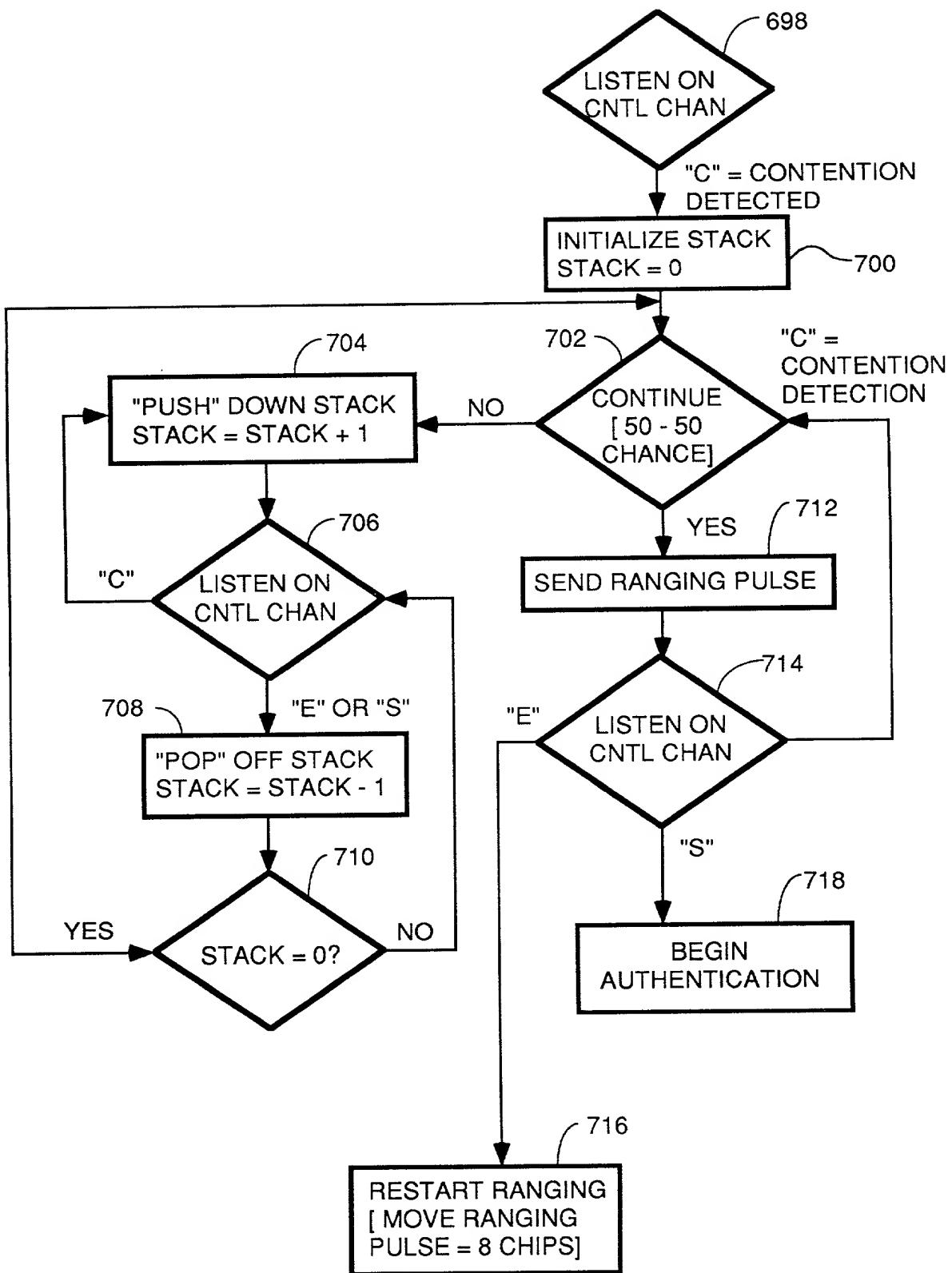
ROUTINE AUTHENTICATION WITH EDGE PULSES





CU RANGING AND CONTENTION RESOLUTION

FIG. 47



CONTENTION RESOLUTION - RU
USING BINARY STACK

FIG. 48

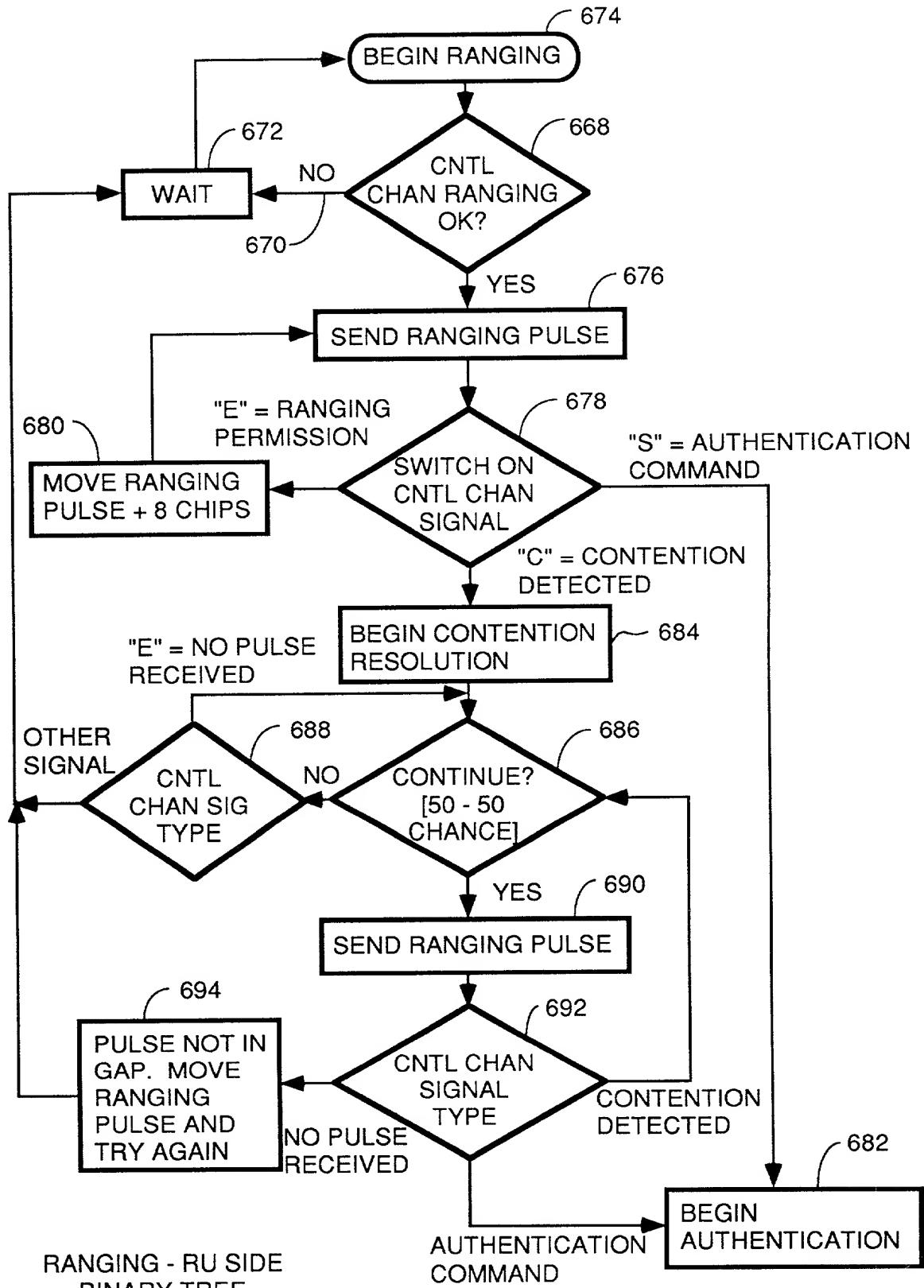


FIG. 49

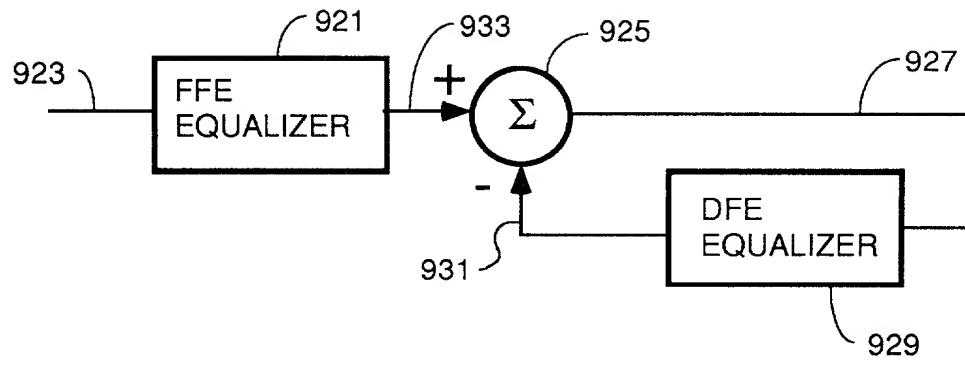


FIG. 50

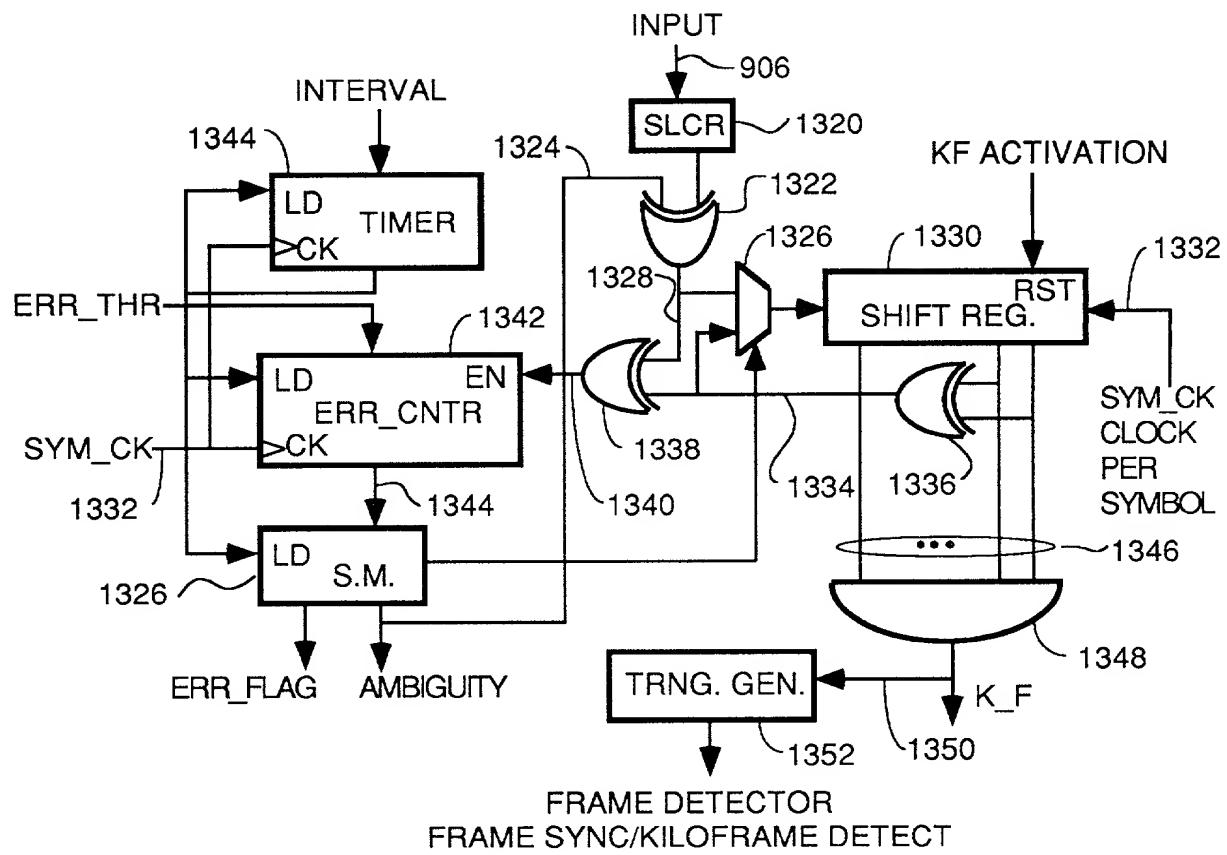
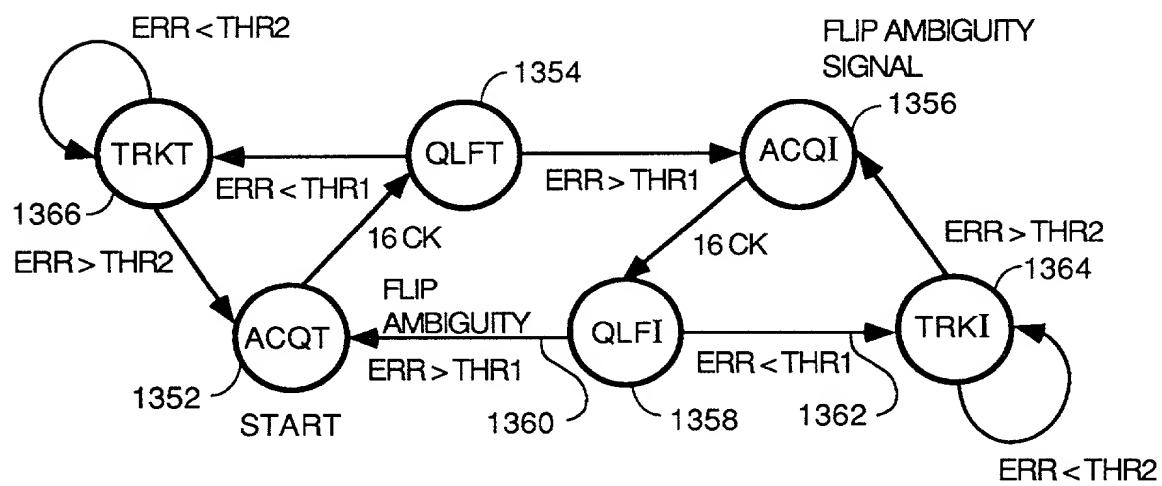


FIG. 51



STATE MACHINE

FIG. 52

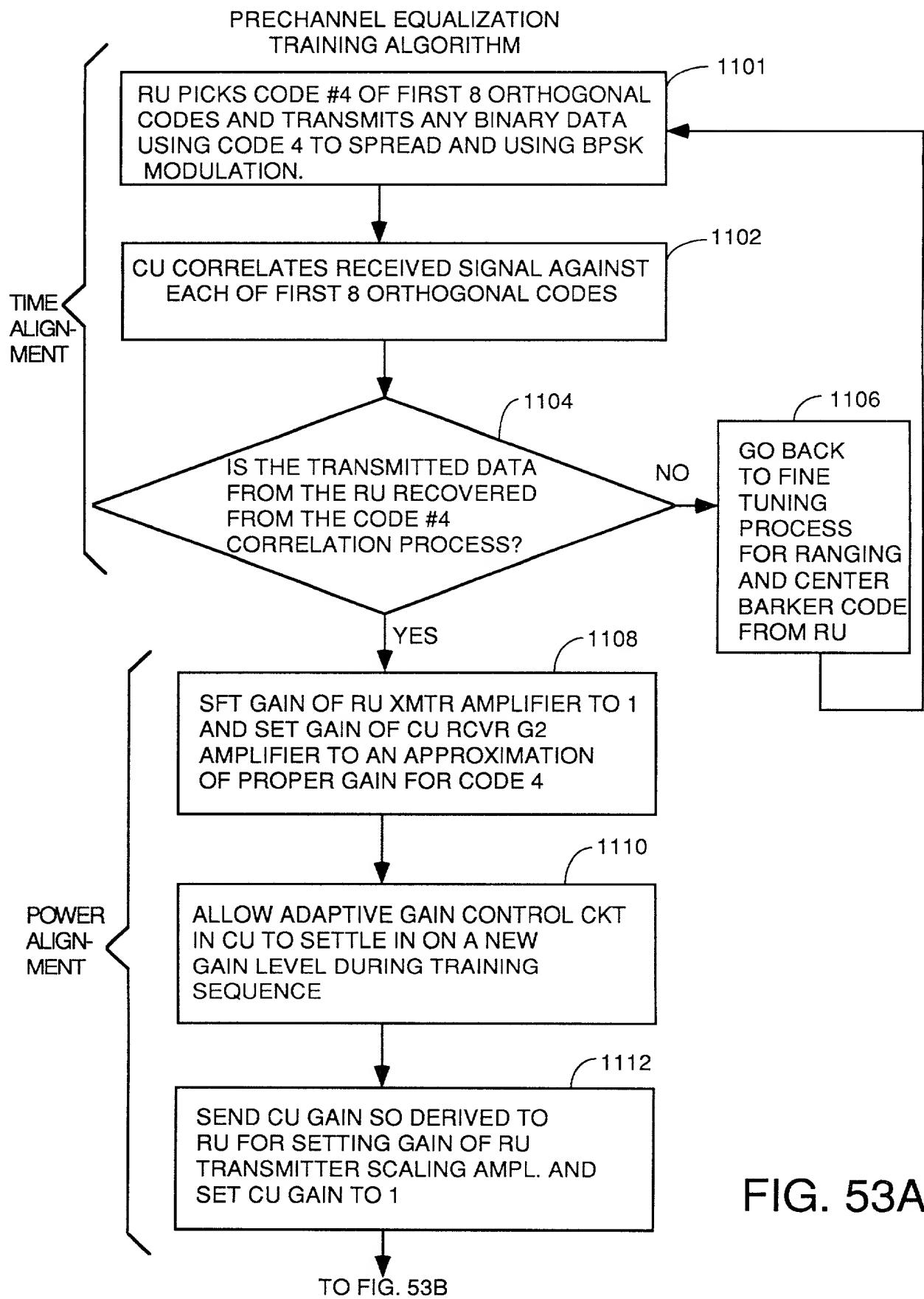


FIG. 53A

UPSTREAM TRAINING & EQUALIZATION

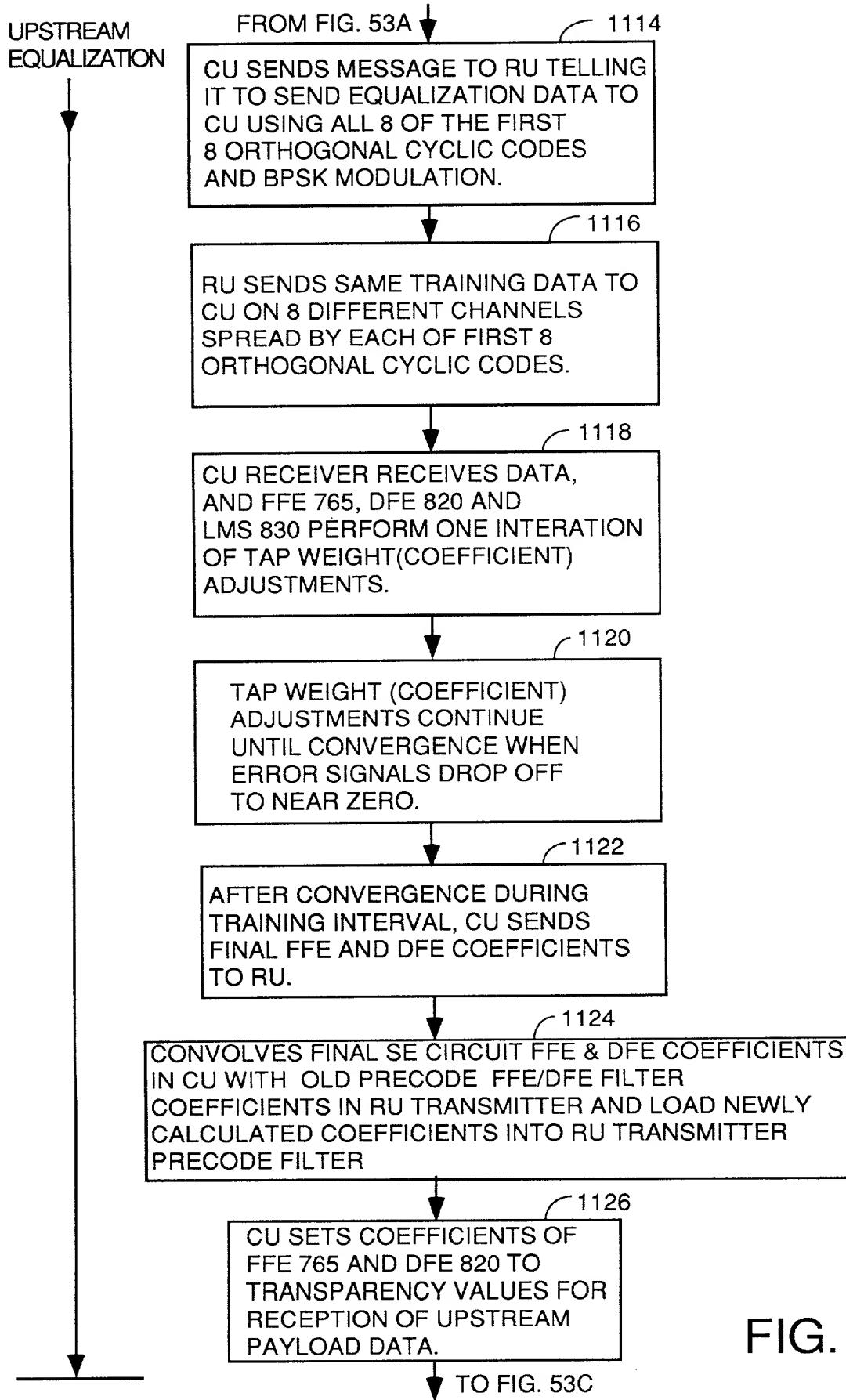


FIG. 53B

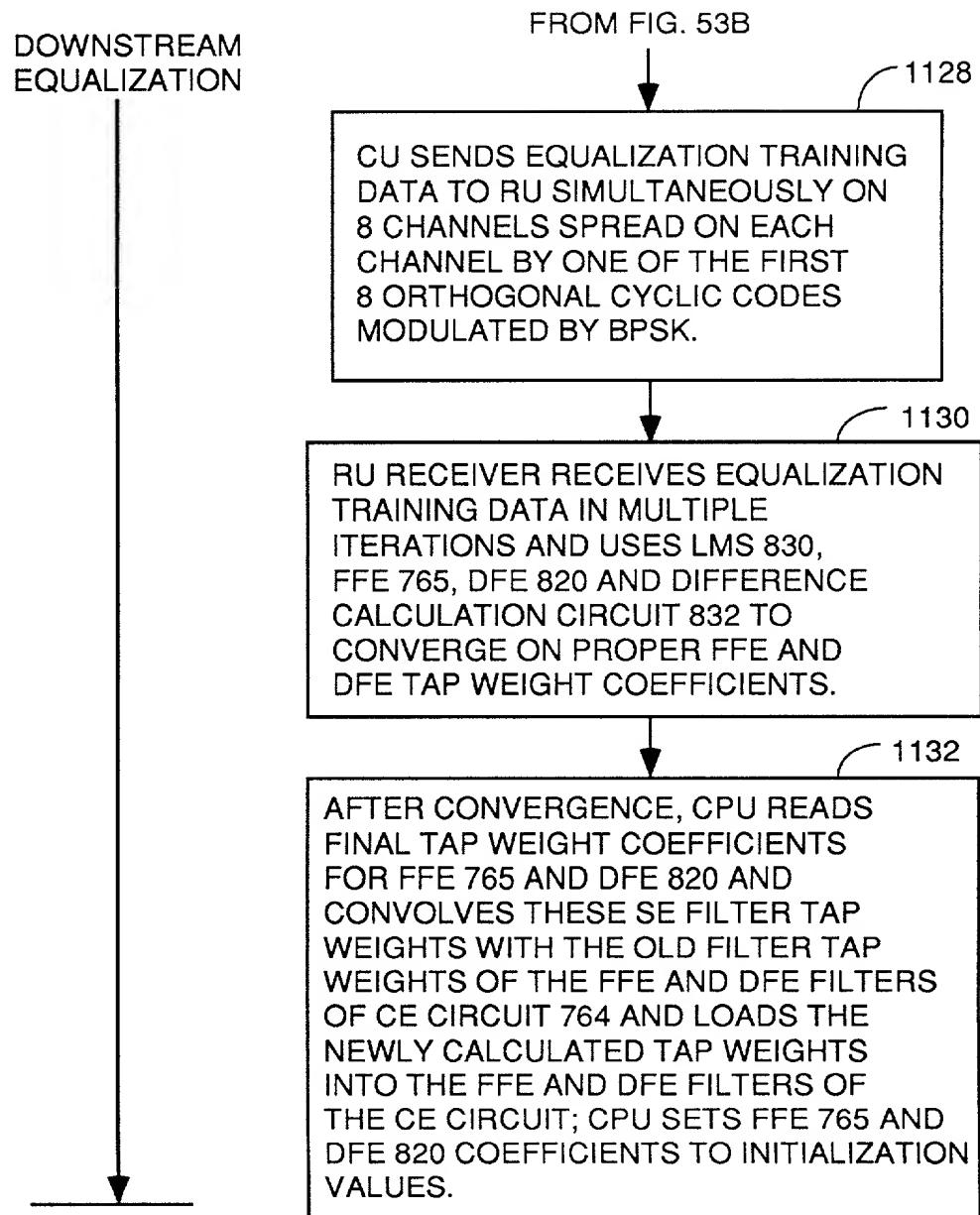
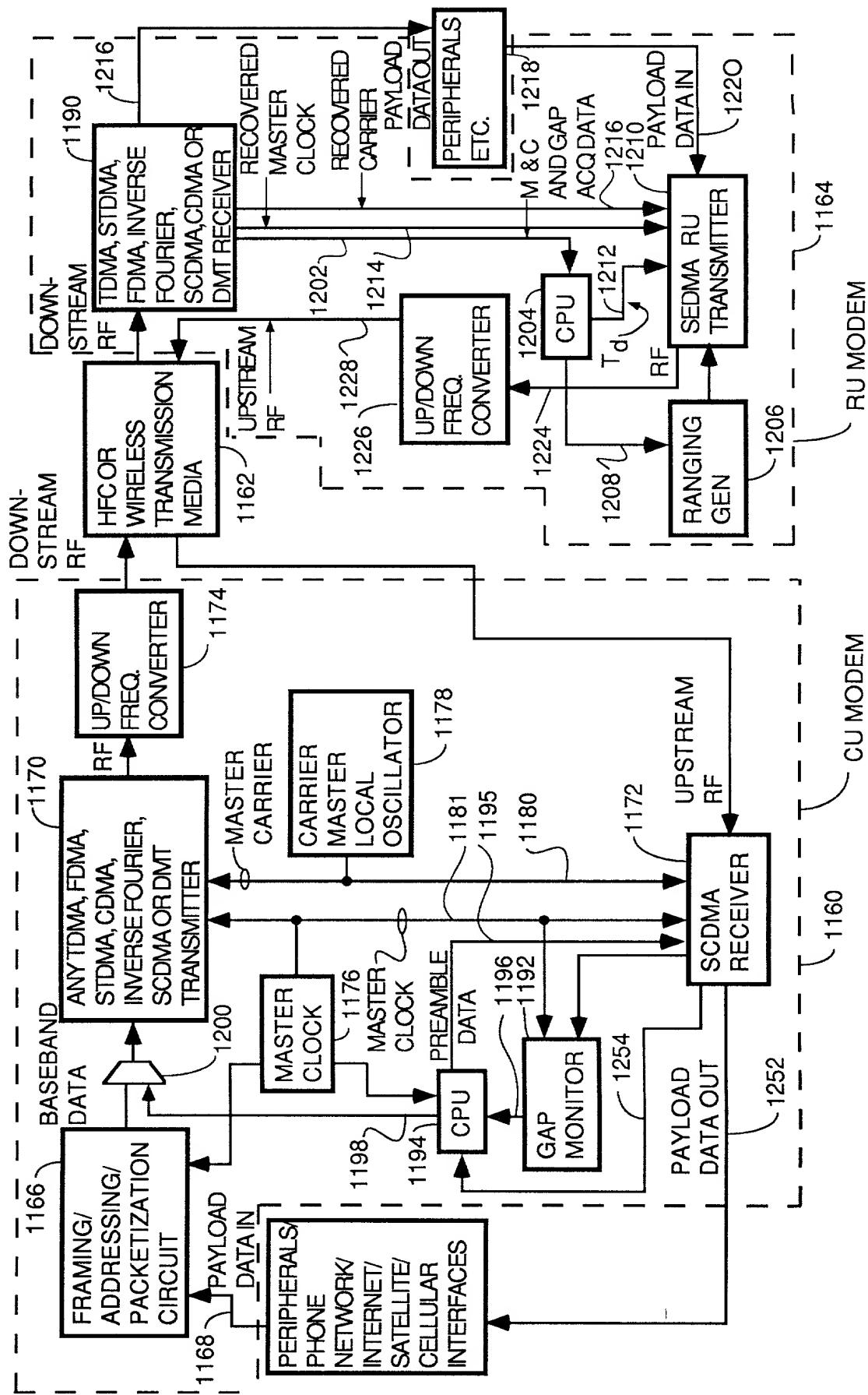
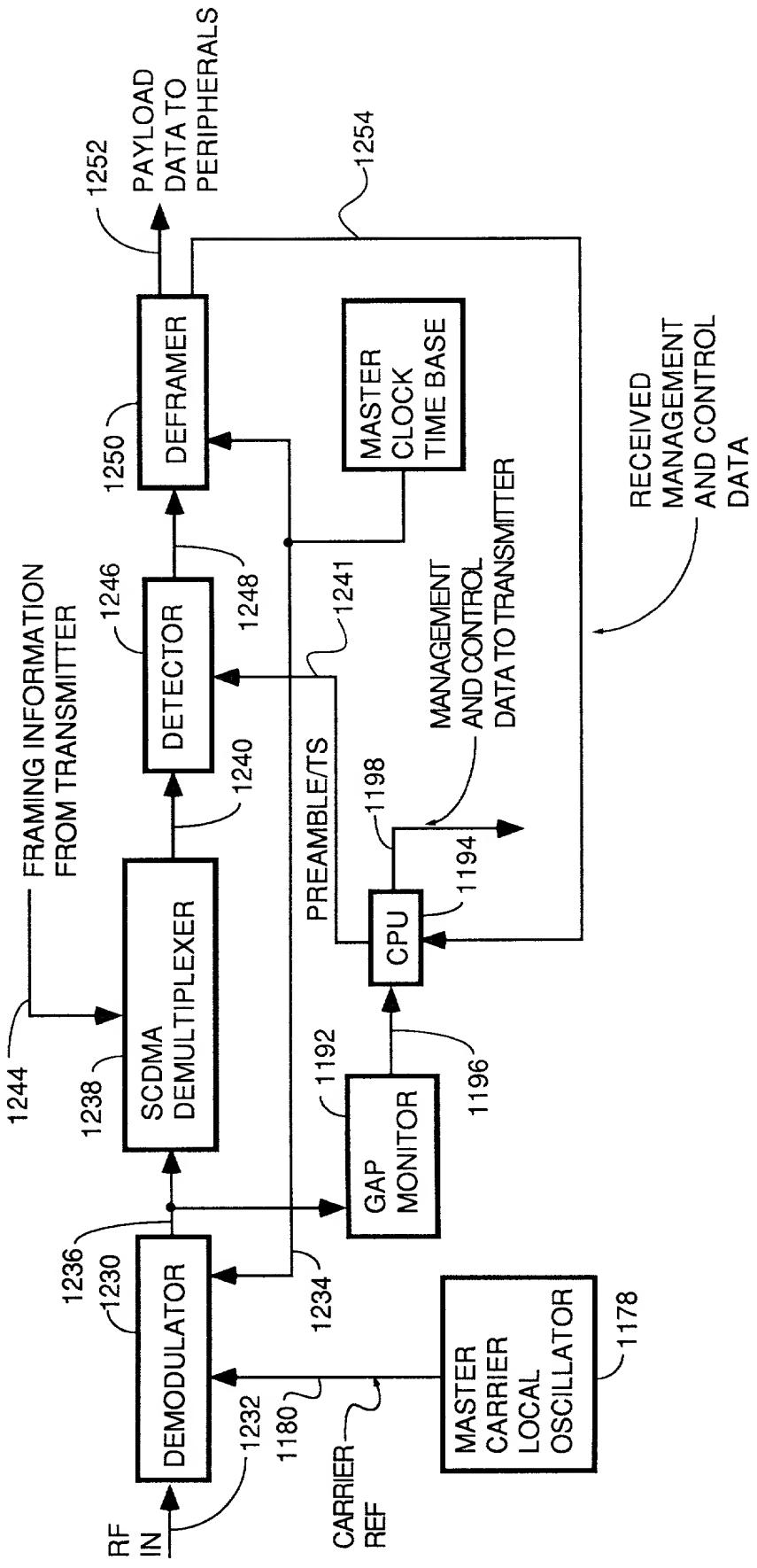


FIG. 53C

FIG. 54





SIMPLE CU SPREAD SPECTRUM RECEIVER

FIG. 55

FIG. 56

SIMPLE RU SPREAD SPECTRUM TRANSMITTER

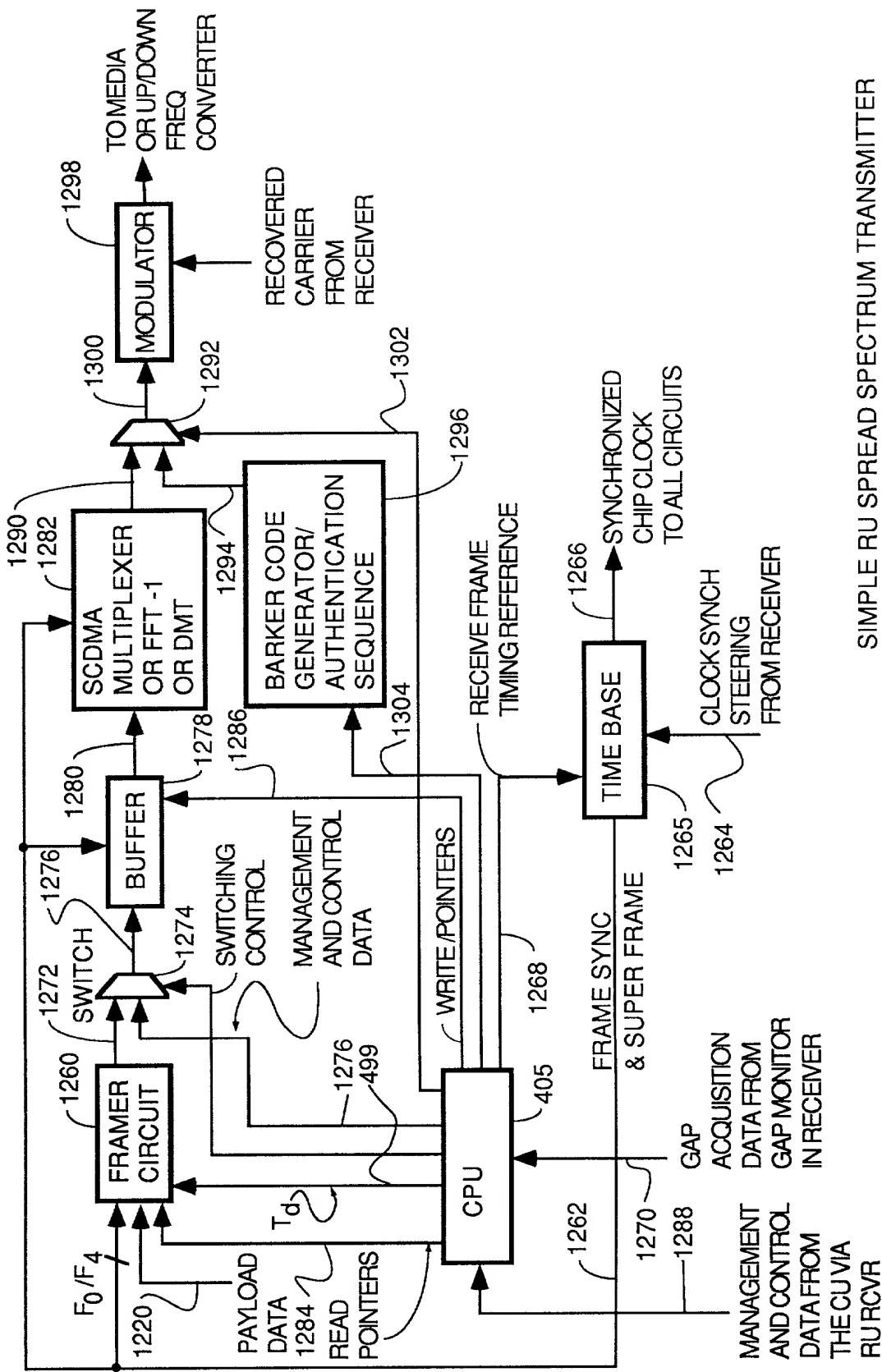
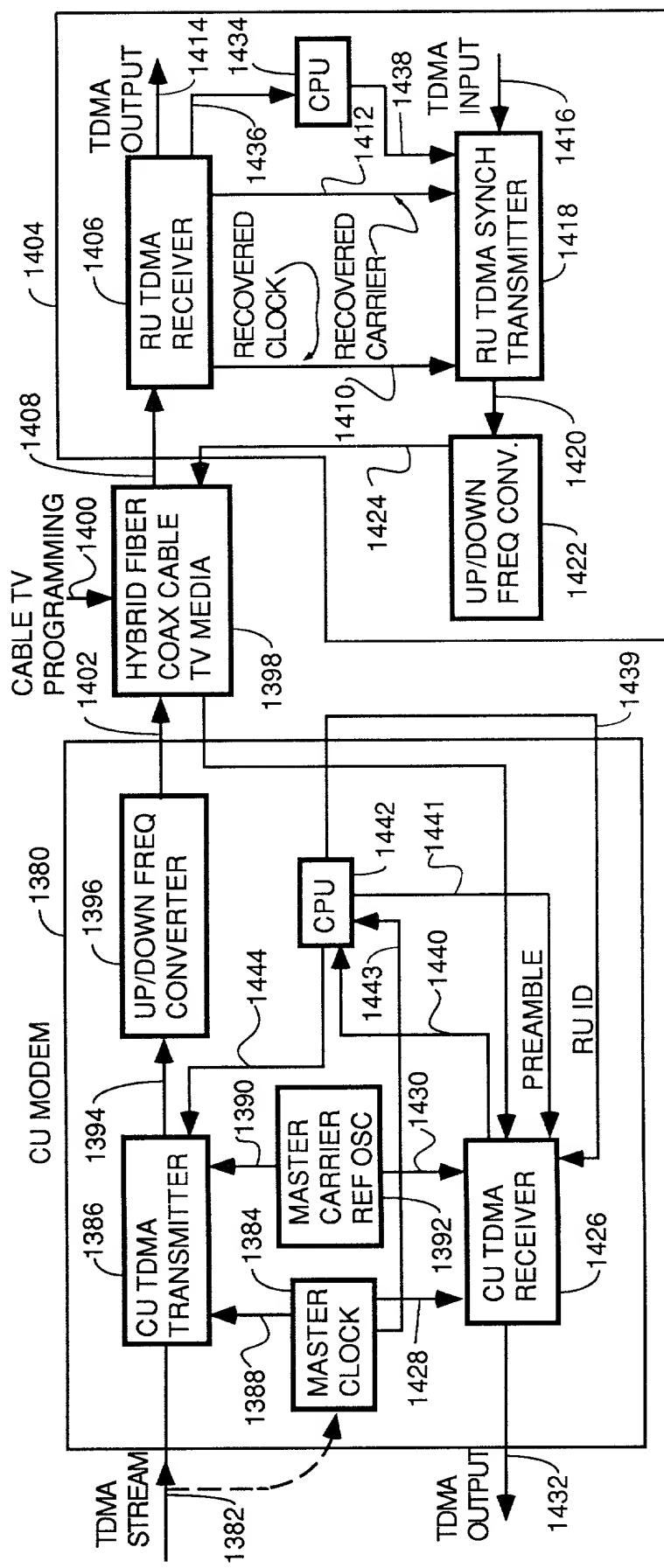


FIG. 57

SYNCHRONOUS TDMA SYSTEM



OFFSET (CHIPS)	1B ASIC		2A ASIC	
	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

TRAINING ALGORITHM

SE FUNCTION

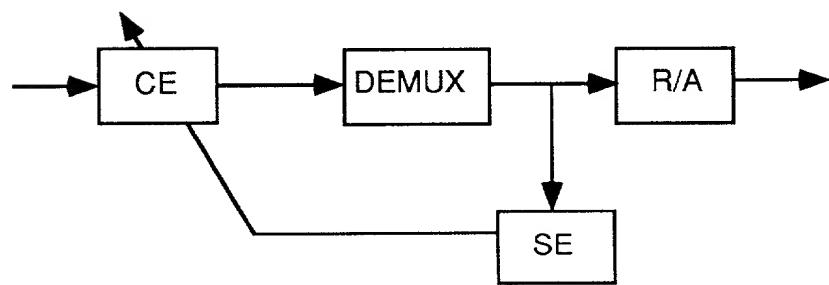
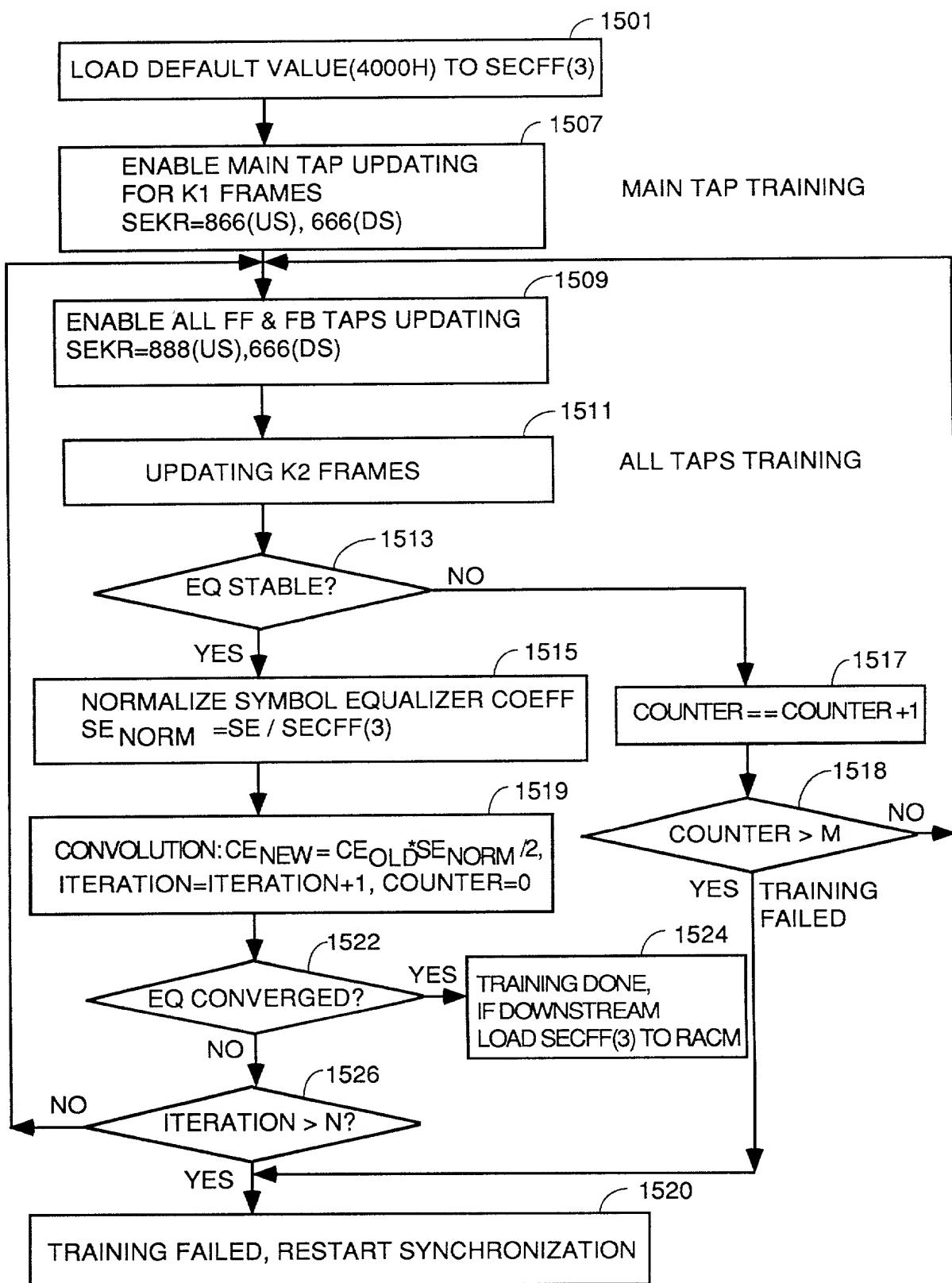


FIG. 59

INITIAL 2-STEP TRAINING ALGORITHM



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

EQ STABILITY CHECK

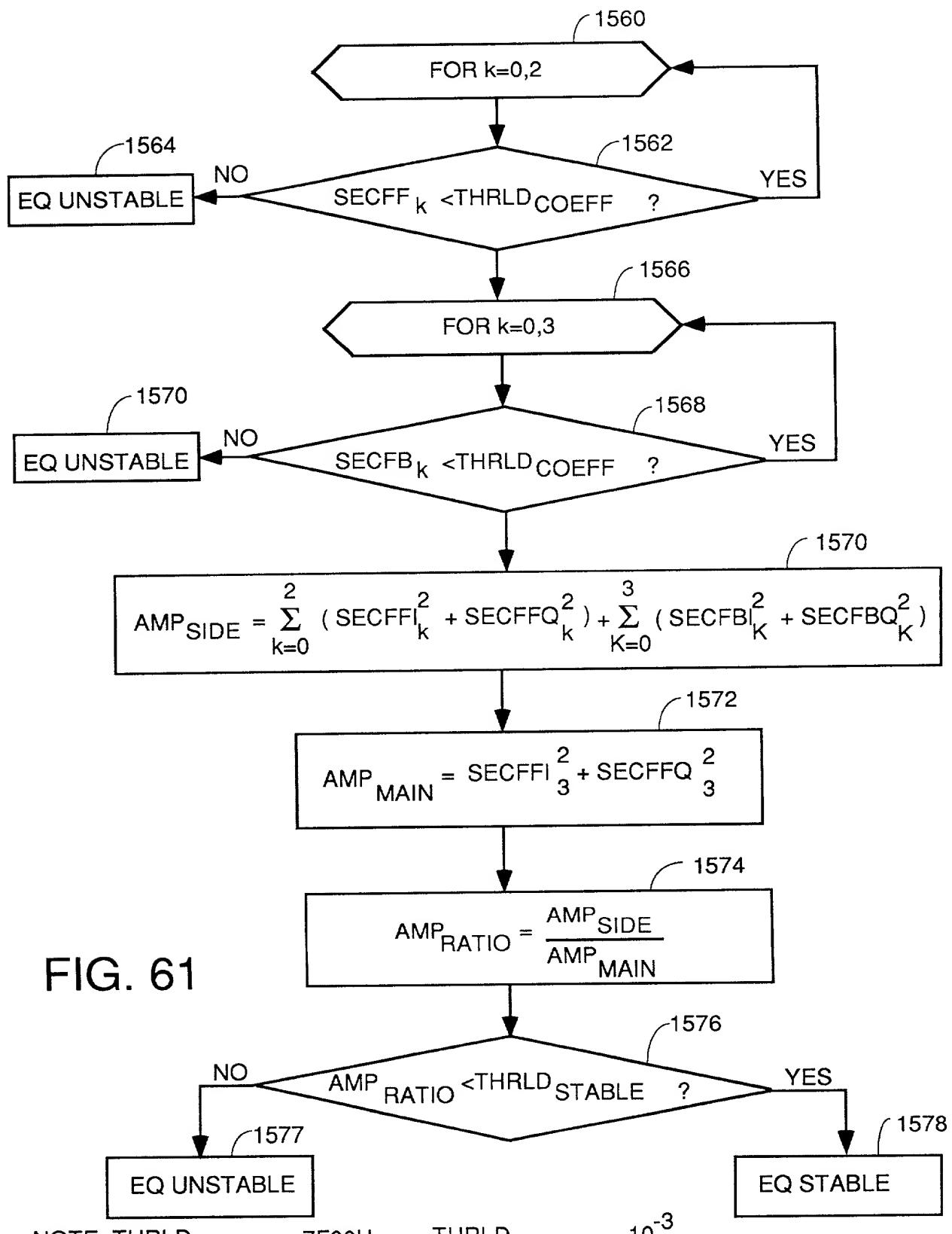


FIG. 61

NOTE: $\text{THRLD COEFF} = 7F00H$

$\text{THRLD STABLE} = 10^{-3}$

PERIODIC 2-STEP TRAINING ALGORITHM

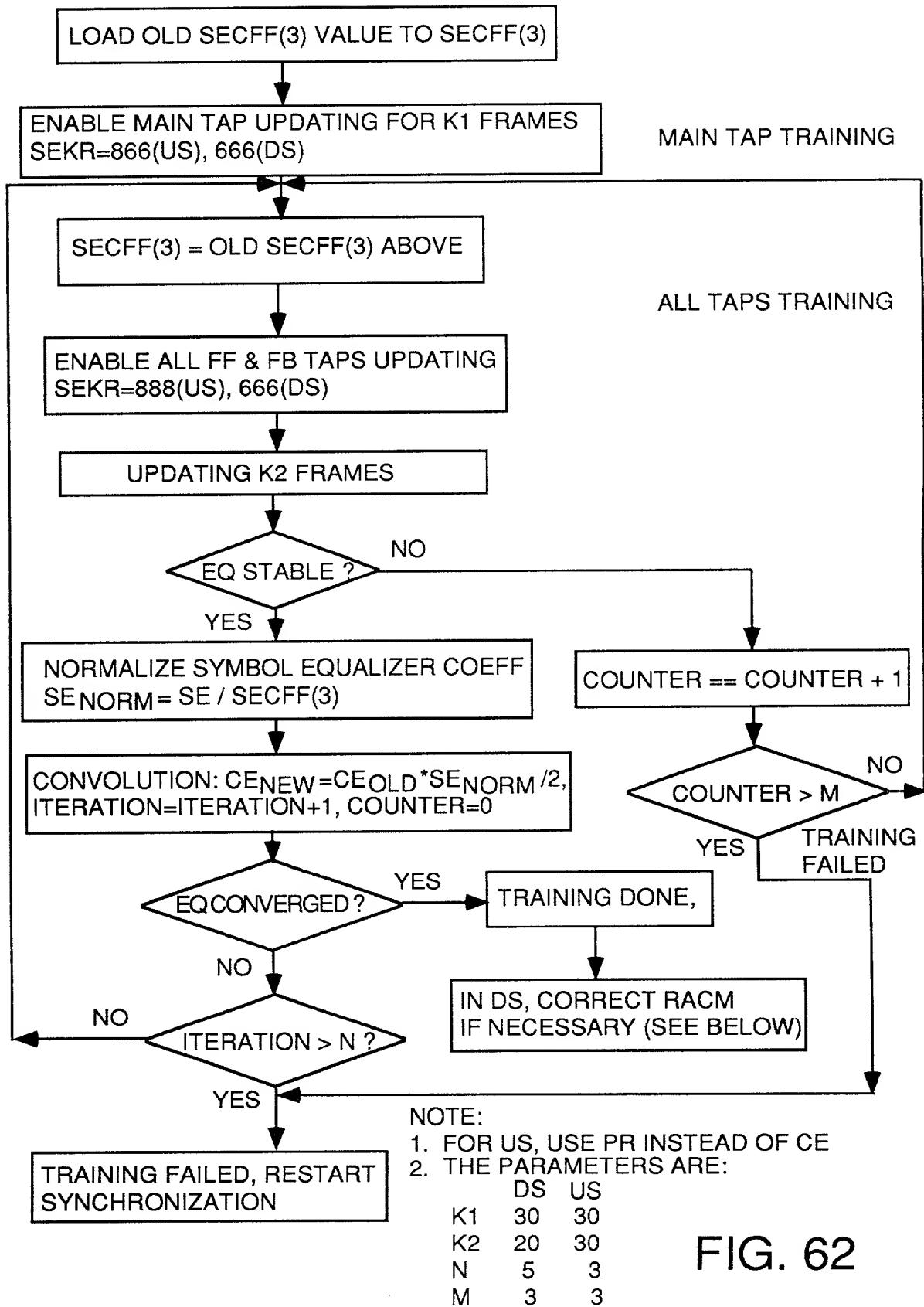
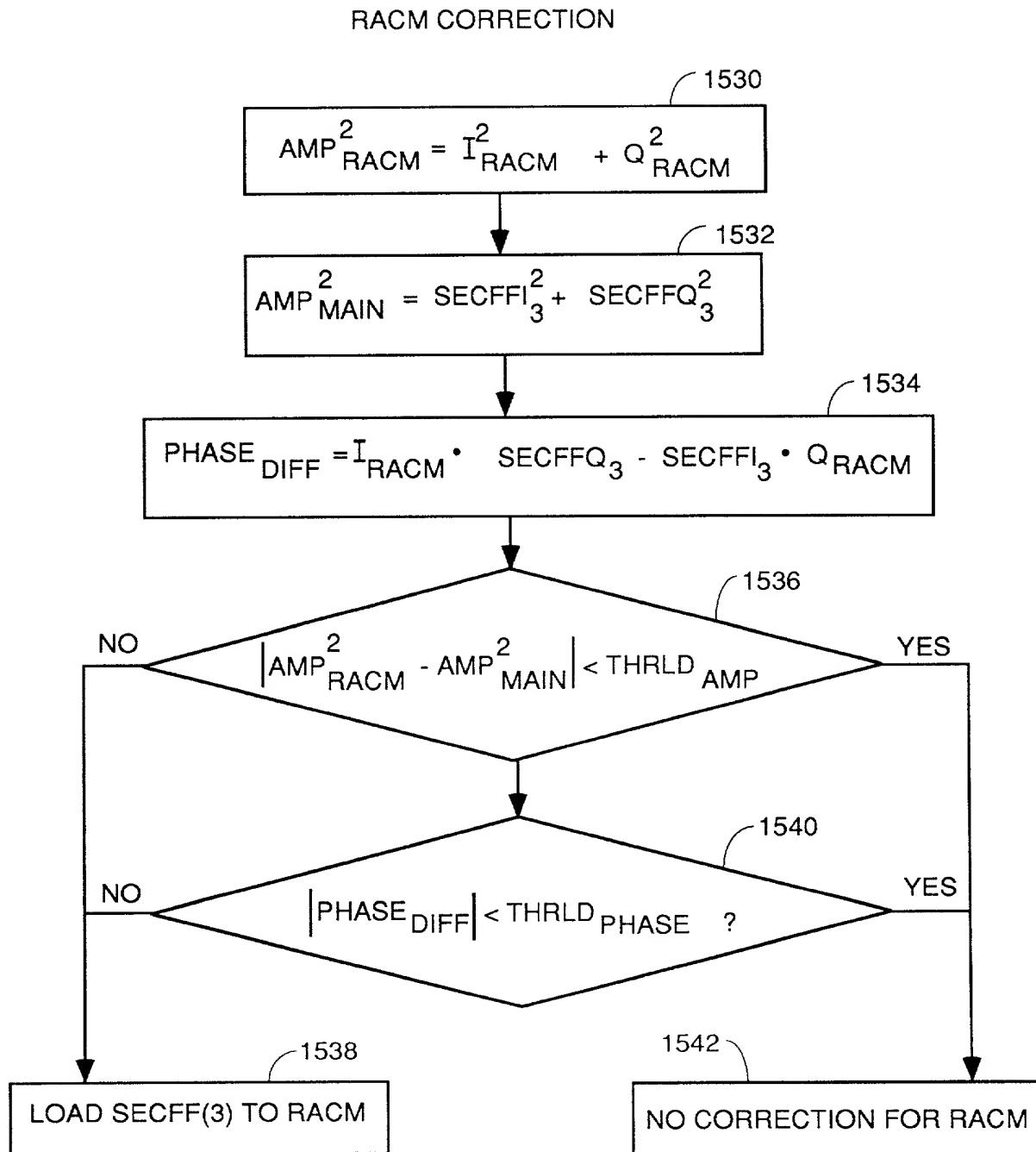


FIG. 62



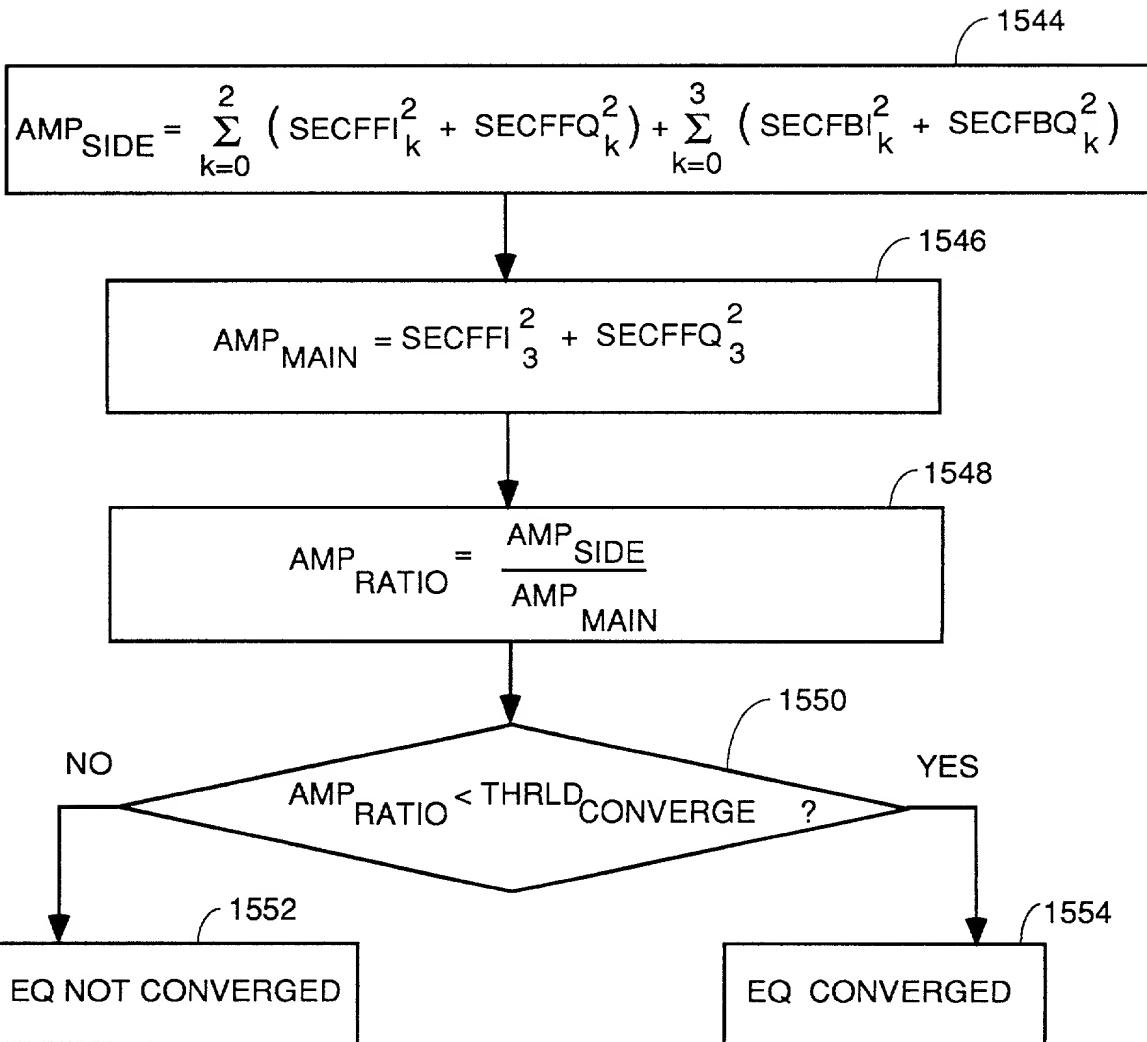
NOTE: $\text{THR LD}_{\text{AMP}} = \text{TBD}$

$\text{THR LD}_{\text{PHASE}} = \text{TBD}$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

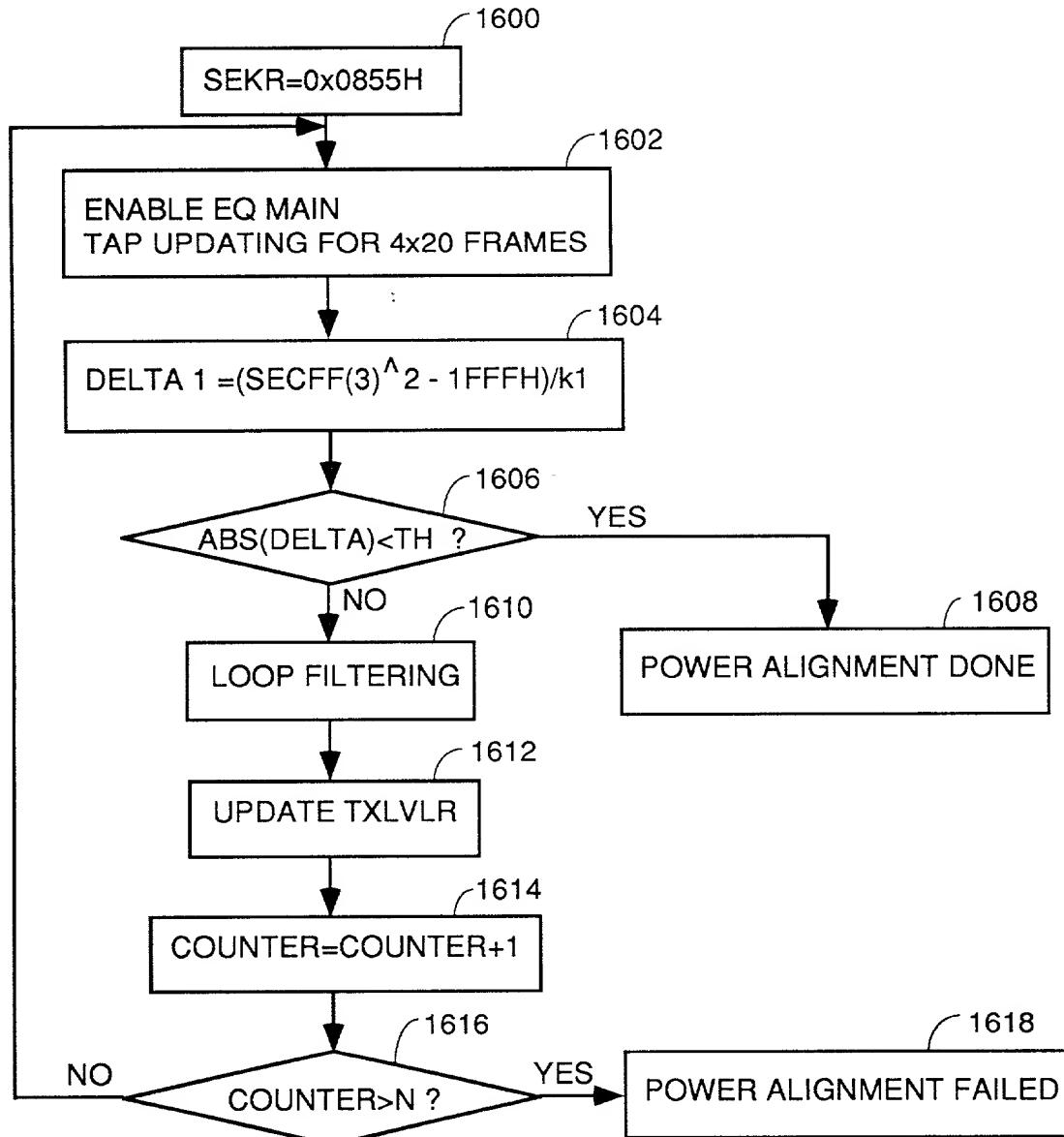
EQ CONVERGENCE CHECK



NOTE: $\text{THRLD}_{\text{CONVERGE}} = 10^{-5}$

FIG. 64

POWER ALIGNMENT FLOW CHART



NOTE: TH = 600H

N = 12

FIG. 65

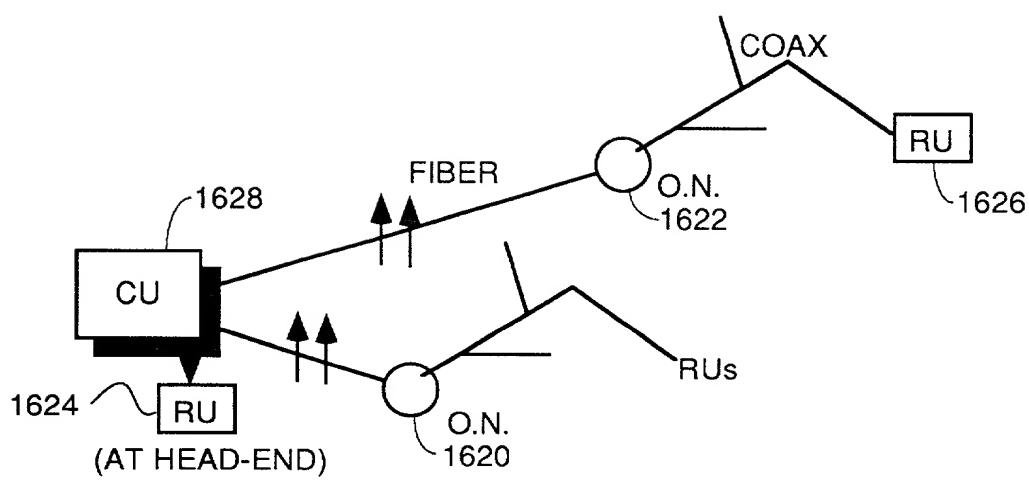
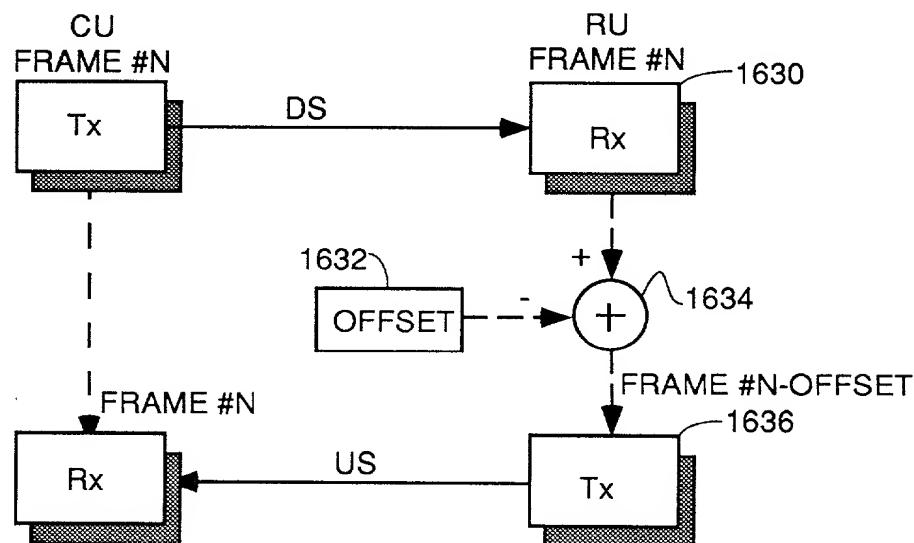


FIG. 66



TOTAL TURN AROUND (TTA) IN FRAMES = OFFSET

FIG. 67

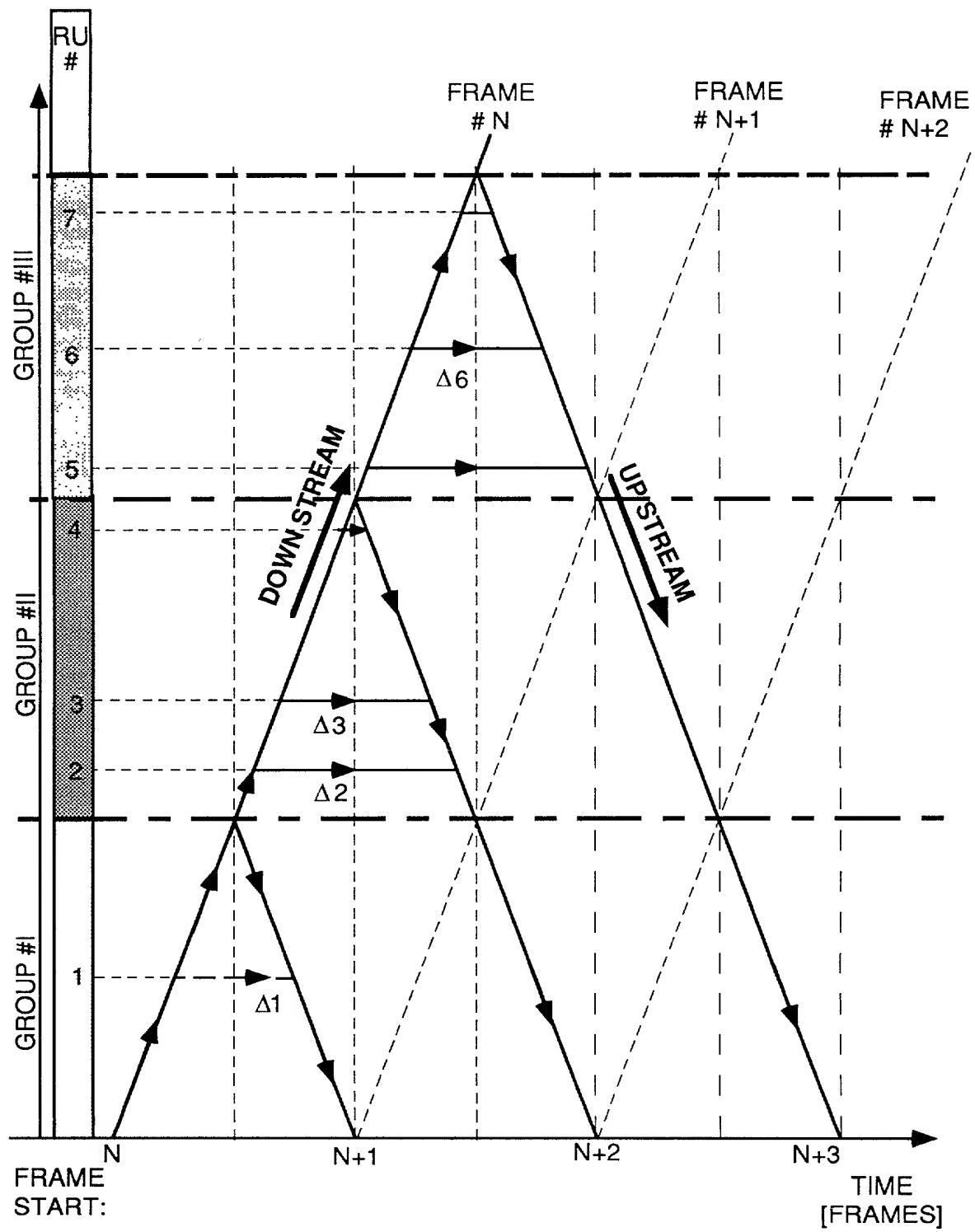
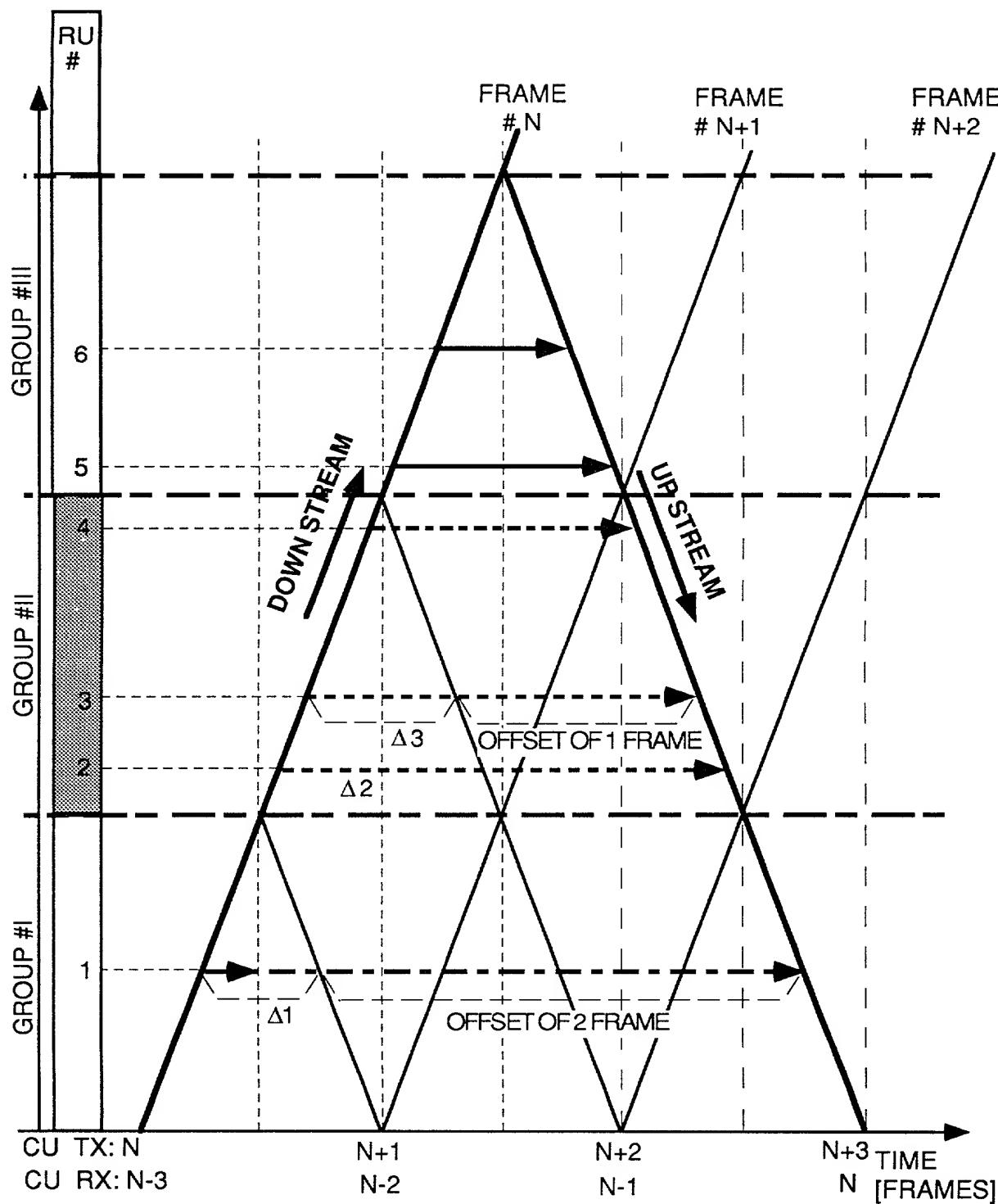


FIG. 68



CONTROL MESSAGE (DOWNSTREAM) AND FUNCTION (UPSTREAM)
PROPAGATION IN A 3 FRAMES TTA CHANNEL

FIG. 69

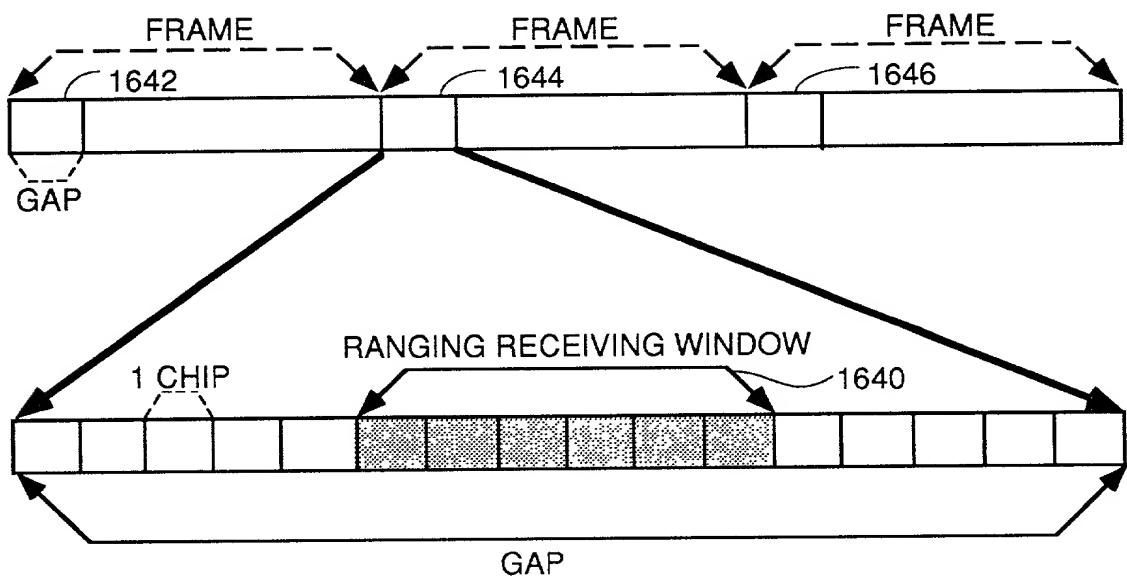
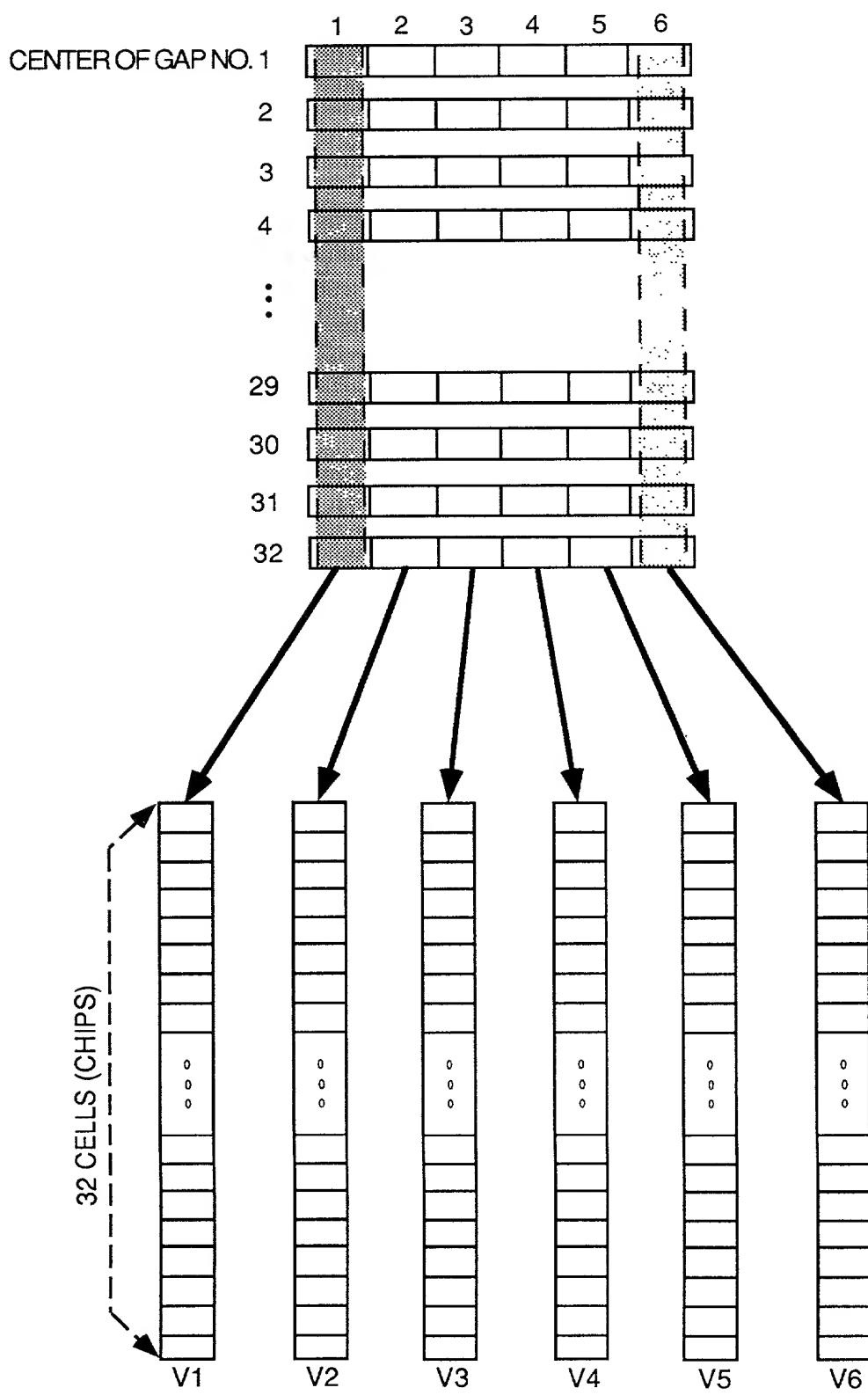


FIG. 70



OVERALL VIEW OF THE CU SENSING WINDOWS
IN A "BOUNDLESS RANGING" ALGORITHM

FIG. 71

CHIP\FR	1	2	3	4	5	6	7		33
1	0	0	1	0	0	1	1	...	0
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72